ER-BK7B1-TM

BK7B1E/F DISK DRIVE TECHNICAL MANUAL

digital equipment corporation • maynard, massachusetts

83323810

CONTROL DATA CORPORATION

CDC® STORAGE MODULE DRIVE

BK7B1-E,F

GENERAL DESCRIPTION
OPERATION
THEORY OF OPERATION
MICROCIRCUITS

HARDWARE REFERENCE MANUAL

REVISION RECORD

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LIST OF EFFECTIVE PAGES

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3-89	A	3-130	A
3-90	A	3-131	A
3-91	A	3-132	A
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3-94	A	3-135	A
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3-97	A	3-138	A
3-98	A	3-139	A
3-99	A	3-140	A
3-100	A	3-141	A
3-101	A	3-142	A
3-102	A	3-143	A
3-103	A	3-144	A
3-104	A	3-145	A
3-105	A	3-146	A
3-106	A	3-147	A
3-107	A	3-148	A
3-108	A	3-149	A
3-109	A	3-150	A
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PREFACE

This manual contains information applicable to the BK7B1E and BK7B1F Storage Module Drives (SMDs). Since this manual covers all the various configurations available on the SMD; it is necessary to understand exactly which configuration you have, in order to know which procedures in this manual are applicable to your drive.

This manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the SMD.

Reference information is provided in three sections in this manual:

- Section 1 - General Description
- Section 2 - Operation
- Section 3 - Theory of Operation

Other manuals, also applicable to the SMD's covered in this manual, are as follows:

Publication No.	Title
83323800	Hardware Maintenance Manual
83323810	Hardware Maintenance Manual
83322440	Normandale Circuits Manual

CONTENTS

FIGURES

TABLES

CONFIGURATION CHART

EQUIPMENT	INPUT VOLTAGES*	TLA NUMBER**
BK7B1E	208 V - 60 Hz	77456058
BK7B1F	220 V - 50 Hz	77456059

*208 V - 60 Hz drives can be rewired for 230 V - 60 Hz.
220 V - 50 Hz drives can be rewired for 240 V - 50 Hz.

**For factory use only.

ABBREVIATIONS

ABR	Absolute Reserve
ABV	Above
ADDR	Address
ADRS	Address
AGC	Automatic Gain Control
AM	Address Mark
AMPL	Amplifier
AMPTD	Amplitude
BLK	Black
BLW	Below
CAR	Cylinder Address Register
CH	Channel
CHAN	Channel
CNTLGL	Centrifugal
CNTR	Counter
COMP	Compensaton
CONFIG	Configuration
CONTD	Continued
CR REF	Cross Reference
CYL	Cylinder
DES	Desired
D/A	Digital to Analog
DCDR	Decoder
DIFF	Difference
DIR	Direction
DLY	Delay
DRV	Drive
DRVR	Driver
DSBL	Disable
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EMER	Emergency
EN	Enable
EOT	End of Travel
EQUIV	Equivalent
FCO	Field Change Order
FCTN	Function
FF	Flip Flop
FIG	Figure

FLT	Fault
FREQ	Frequency
FTU	Field Test Unit
FWD	Forward
GEN	Generator
GND	Ground
HD	Head
I/O	Input-Output
INTLK	Interlock
INTGRTR	Integrator
LD	Load
MAINT	Maintenance
MAX	Maximum
MB	Megabyte
MFM	Modified Frequency Modulation
MK	Mark
MULT	Multiple
NC	No Connection
NEG	Negative
NOM	Nominal
NORM	Normal
NRM	Normal
NRZ	Nonreturn to Zero
PC PT	Piece Part
PLO	Phase Lock Oscillator
PN	Part Number
POS	Positive
PWR	Power
RCVRS	Receivers
RD	Read
RDY	Ready
REC	Receiver
REF	Reference
REG	Register
REV	Reverse
RGTR	Register
TRM	Reserve Timer
RTZ	Return to Zero
S&IOBC	Sector and Index on B Cable
S/C	Series Code
SEC	Second
SEL	Select
SEQ	Sequence
SER	Servo
SH	Sheet
SOL	Solenoid

SR	Servo
SW	Switch
T	Track
TBS	To Be Supplied
TLA	Top Level Assembly
TP	Test Point
TRK	Track
TTL	Transistor Transistor Logic
UNREG	Unregulated
VCO	Voltage Controlled Oscillator
W+R	Write or Read
W•R	Write and Read
W/	With
W/O	Without
WRT	Write
WT	White
XDUCER	Transducer
XMTR	Transmitter

GENERAL DESCRIPTION

SECTION 1

INTRODUCTION

The Control Data Storage Module Drives (SMD's) are high speed, random access digital data storage devices that connect to a central processor through a controller. The total data storage capacity of the units is 300 megabytes. All the equipment specifications for each drive are listed in table 1-1.

The remainder of this section provides a general description of the drive and is divided into the following areas:

- Drive Functions - Explains the major functional areas of the drive.
- Drive Physical Description - Provides description of the drives physical characteristics.
- Equipment Configuration - Describes the various drive configurations and how to identify them.

DRIVE FUNCTIONAL DESCRIPTION

GENERAL

The major functional areas of the drive are shown on figure 1-1 and described in the following paragraphs. More detailed descriptions of each of the following areas is found in section 3 of this manual (Theory of Operation).

The disk pack is the recording medium for the drive. The disk pack consists of ten, 14-inch disks, center mounted on a hub. The recording surface of each disk is coated with a layer of magnetic oxide and related binders and adhesives.

There are nineteen recording surfaces and one servo surface. The servo surface contains prerecorded information that is used by the servo circuits to position the heads at the desired area on the disk pack.

TABLE 1-1. EQUIPMENT SPECIFICATIONS

Specification	Value
Size	
Height	920 mm (36 in)
Width	914 mm (36 in)
Depth	584 mm (23 in)
Weight	252 kg (550 lbs)
Temperature	
Operating	15.5 °C (59° F) to 32.2° C (90° F)
Operating Change/Hr	6.6° C (12° F) per hr
Transit (packed for shipment)	-40.4° C (-40° F) to 70° C (158° F)
Non-Operating Change/Hr	20° C (36° F) per hr
Relative Humidity	
Operating	20% to 80% No Condensation
Transit (packed for shipment)	5% to 95% No Condensation
Altitude	
Operating	-305 m (-1000 ft) to 2000 m (6500 ft)
Transit (packed for shipment)	-305 m (-1000 ft) to 4572 m (15 000 ft)
Disk Pack	
Type	883-91 (one per drive)
Disks/Pack	12 (Top and bottom disks are for protection only.)
Data Surfaces	19
Servo Surfaces	1
Usable Tracks/Surface	823
Tracks/Inch	384
Track Spacing (center to center)	0.0666 mm (0.0026 in)
Coating	Magnetic Oxide
Data Capacity	300 MB
Bytes/Track	20 160
Bytes/Cylinder	383 040
Bytes/Spindle	309 496 320
Cylinders/Spindle	823
	NOTE: Based on 8 bit bytes not allowing for tolerance gaps for sectoring etc.

Table Continued on Next Page

TABLE 1-1. EQUIPMENT SPECIFICATIONS (Contd)

Specification	Value
Recording Characteristics	
Mode	Modified Frequency Modulation (MFM)
Density (nominal)	
Outer Track	4038 bits/in
Inner Track	6038 bits/in
Rate (nominal)	9.67 MHz (1 209 600 bytes/sec)
Heads	
Read/Write	19
Servo	1
Read/Write Width	0.051 mm (0.002 in)
Seek Characteristics	
Mechanism	Voice Coil, Driven By Servo Loop
Max Seek Time (411 or 823 Tracks)	55 ms
Max Track Seek Time	6 ms
Average Seek Time	30 ms
Latency	
Average	8.33 ms (at 3600 r/min)
Maximum	17.3 ms (at 3474 r/min) NOTE: Latency is time required to reach specific track location after drive is on cylinder.
Spindle Speed	3600 r/min
Controllers Per Drive	Refer to Configuration Chart in front matter of this manual.
Input Voltages	Refer to Configuration Chart in front matter of this manual.

The recording surfaces are used for data storage. Each of these furfaces has its recording tracks grouped in a 2 inch band near the outer edge of the disk. The number of tracks contained on each recording surface and the spacing between the tracks is found in table 1-1.

The disk pack is portable and is interchangeable between drives. Both the BK6XX and BK7XX use the same type of disk pack.

POWER SYSTEM

The drive has its own self contained power supply which receives its input from the site main power source. The power supply provides all the voltages necessary for drive operation.

INTERFACE

The drive can communicate only with the controller. The controller issues all commands to the drive, which decodes the commands and initiates the proper operation. In addition to the commands, the controller sends write data, write clock and power sequence information to the drive.

The drive sends various status signals, read data, read clock, and servo clock information to the controller. These signals are used by the controller to monitor and control operations performed by the drive.

SEEKING

The drive must position the heads over the desired data record before it writes or reads data. This function is called seeking and it is performed by a servo system consisting of control logic and a head positioning mechanism.

READING AND WRITING

The drive is capable of both writing data on and reading it from the disk pack. During a write operation, the drive receives data from the controller, processes it and writes it on the disk pack. During a rad operation, the drive recovers data from the disk pack, and transmits it to the controller.

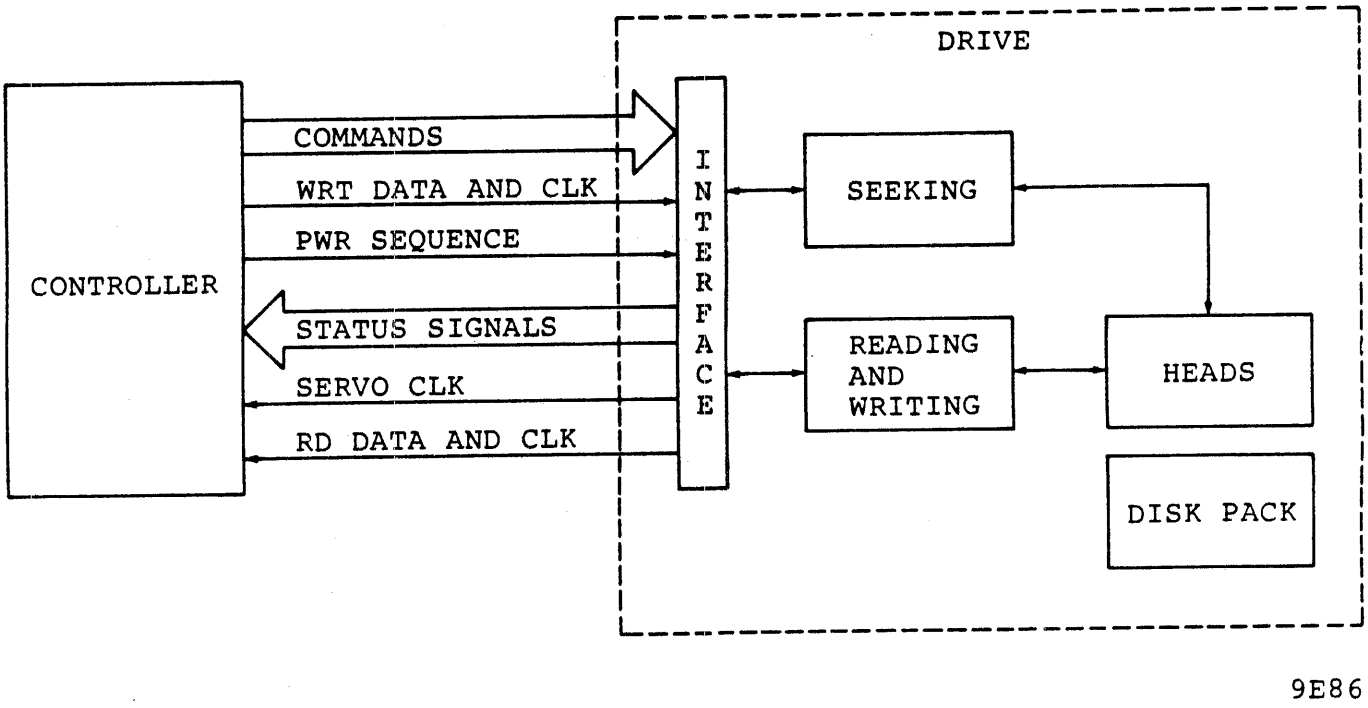


Figure 1-1. Drive Functional Blocks

DRIVE PHYSICAL DESCRIPTION

GENERAL

The following describes the physical characteristics of the drive. The discussion is divided into two major areas (1) assemblies and (2) logic and circuitry.

ASSEMBLIES

The major drive assemblies are shown on figure 1-2 and described in table 1-2. A more complete description of the drive assemblies is found in the Parts Data section of the maintenance manual.

LOGIC AND CIRCUITRY

The drive contains integrated and discrete component circuits as well as relays, switches and other electromechanical elements. All of these work together in performing the various drive functions.

Diagrams showing all circuits and interconnecting wiring are contained in the maintenance manual. Sections 5 and 6 of this manual describe characteristics of individual discrete and integrated circuits.

EQUIPMENT CONFIGURATION

GENERAL

The equipment configuration is identified by the equipment identification plate and by the FCO log. It is necessary to identify the equipment configuration to determine if the manuals being used are applicable to the equipment. The following describes the cabinet identification plate, FCO log and manual to equipment correlation.

EQUIPMENT IDENTIFICATION PLATE

General

This plate is attached to the frame at the rear of the drive (refer to figure 1-3). This plate identifies the drives basic mechanical and logical configuration at the time it leaves the factory. The information contained on this plate is defined in the following.

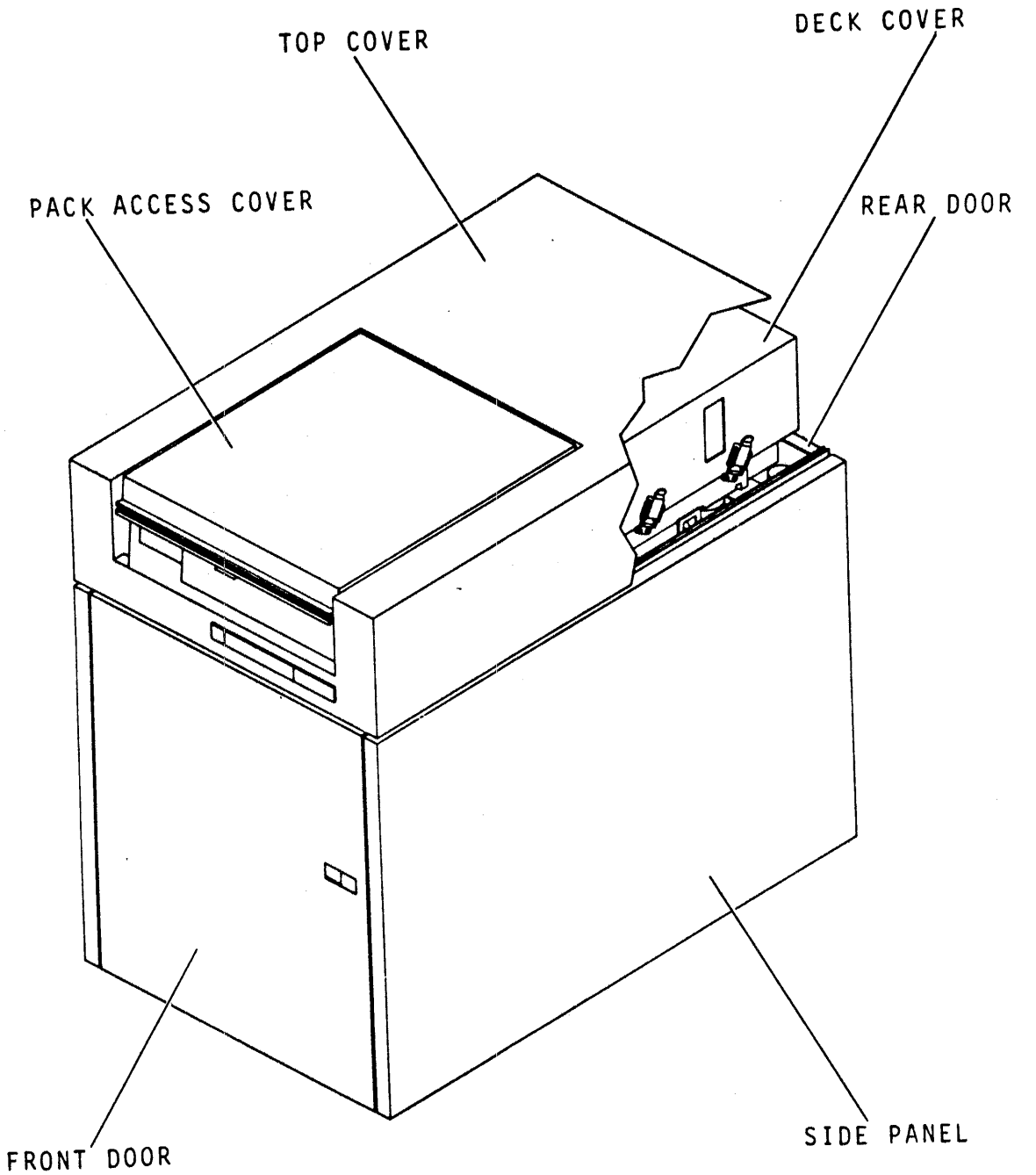


Figure 1-2. Drive Assemblies (Sheet 1 of 2)

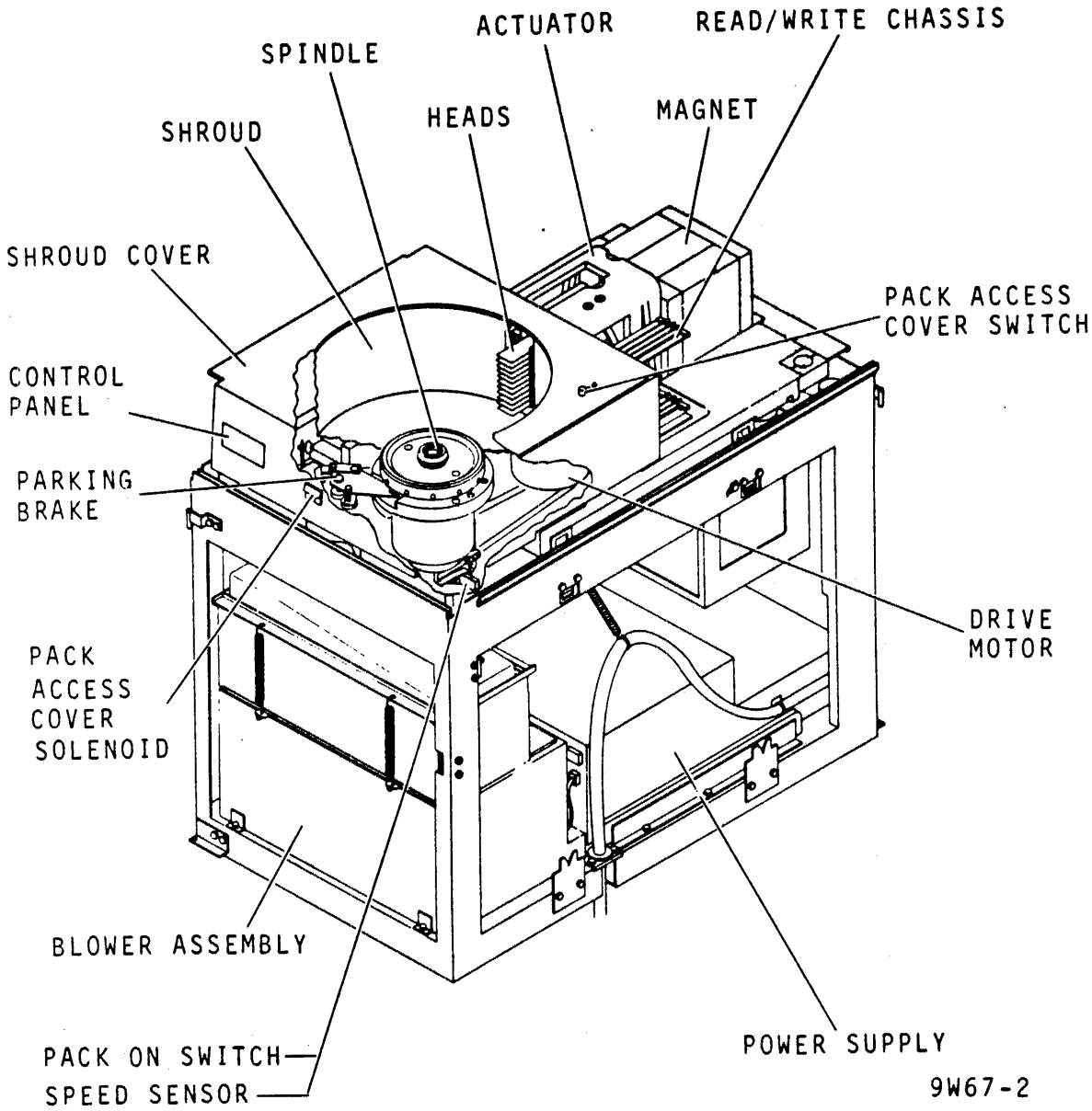


Figure 1-2. Drive Assemblies (Sheet 2 of 2)

TABLE 1-2. DRIVE ASSEMBLIES

Actuator	Contains voice coil and carriage. This assembly positions the heads over the disk pack.
Blower Assembly	Contains a blower motor that circulates cooling air for the drive.
Deck Cover	Provides an electrical interference shield for the drive and also reduces noise level output from drive.
Drive Motor	Provides rotational motion that turns spindle and disk pack.
Front Door	Provides access to blower assembly and the lower front part of cabinet.
Heads	Detect data transitions that are on the pack if drive is reading. Writes data transitions on the disk pack if drive is writing.
Logic Chassis	Contains logic cards that control operation of drive.
Magnet	Provides permanent magnetic field that is used in conjunction with voice coil to move carriage and heads.
Operator Control Panel	Contains switches that allow operator to control and monitor basic operation of drive.
Pack Access Cover	Provides access to disk pack and pack area.
Pack Access Cover Solenoid	Prevents pack access cover from being opened if the pack is spinning.
Pack Access Cover Switch	Interlock that de-energizes drive motor if pack access cover is opened while pack is spinning. It also prevents motor from starting unless cover is closed.

Table Continued on Next Page

TABLE 1-2. DRIVE ASSEMBLIES (Contd)

Pack On Switch	Interlock that prevents drive motor from starting when pack is not installed.
Parking Brake	Holds spindle while disk pack is being installed and removed.
Power Supply	Furnishes all necessary voltages for drive operation.
Read/Write Chassis	Contains cards that are essential to drive read/write operations.
Rear Door	Provides access to power supply, logic chassis and lower rear of cabinet.
Shroud and Shroud Cover	Provides protection and ventiliation for disk pack.
Side Panels	Provide access to either side of drive.
Spindle and Lockshaft	Provides mounting surface for disk pack. Lockshaft secures disk pack to spindle. Drive motor transmits rotational motion to spindle via drive belt thereby causing disk pack to rotate.
Top Cover	Covers entire top of drive thereby protecting drive assemblies and reducing output noise level.

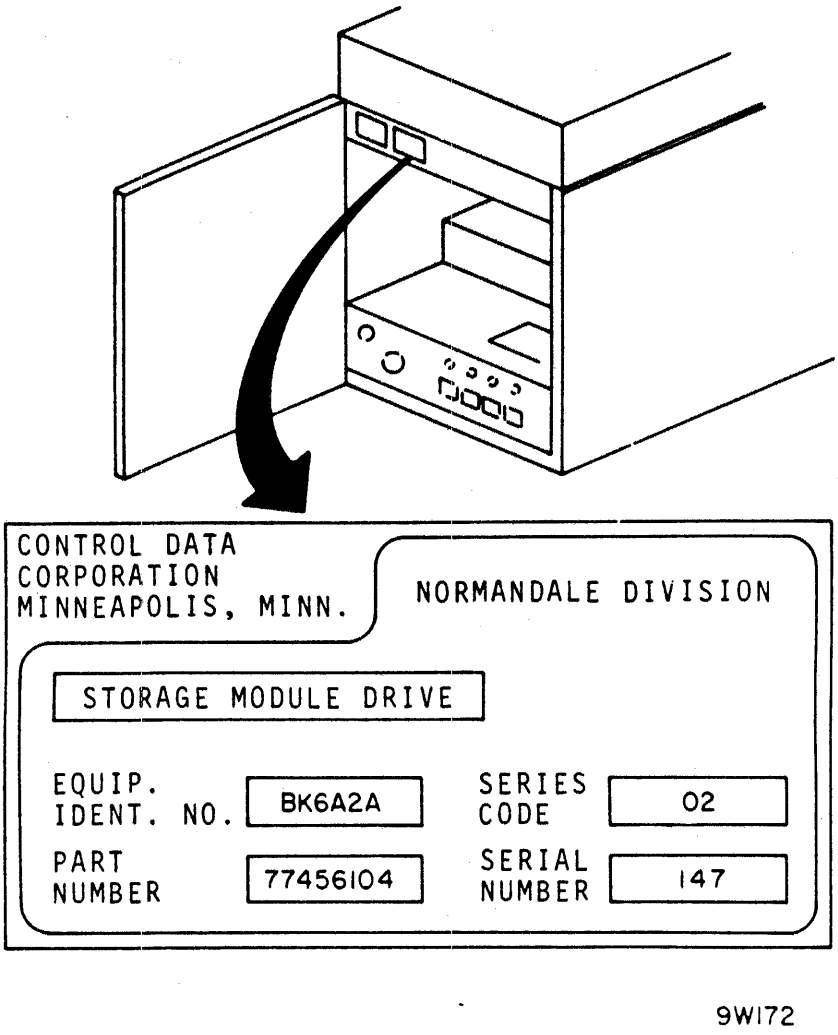
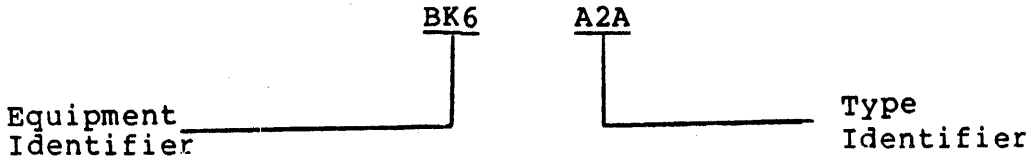


Figure 1-3. Equipment Identification Plate

Equipment Identification Number

This number is divided into the two parts shown in the example:

EXAMPLE:



The equipment identifier indicates the basic functional capabilities of the drive. This number will be either BK6 or BK7. The differences between these units can be determined by referring to table 1-1.

The type identifier indicates differences between drives that have the same equipment number. These differences are necessary to adapt a drive to specific system requirements. However, they do not change the overall capabilities of the drive as defined in table 1-1.

Series Code

The series code represents a time period within which a unit is built. While all units are interchangeable at the system level, regardless of series code, parts differences may exist within units built in different series codes. When a parts difference exists, that difference is noted in the parts data section of maintenance manual volume 1.

Part Number

This number indicates the top level assembly number of the equipment and is for factory use only.

Serial Number

Each drive has a unique serial number assigned to it. Serial numbers are sequentially within a family of drives. Therefore, not two equipments will have the same serial number.

FCO LOG

Field Change Orders (FCO's) are electrical or mechanical changes that may be performed either at the factory or in the field. FCO changes do not affect the series code but are indicated by an entry on the FCO log that accompanies each machine. The components of a machine with an FCO installed may not be interchangeable with those of a machine without the FCO; therefore, it is important that the FCO log be kept current by the person installing each FCO.

MANUAL TO EQUIPMENT CORRELATION

Throughout the life cycle of a machine, changes are made either in the factory build (a series code change) or by FCOs installed in the field. All of these changes are also reflected in changes to the manual package.

In order to assure that the manual correlates with the machine, refer to the Manual To Equipment Correlation sheet located in the front matter of the hardware maintenance manual. This sheet records all the FCOs which are reflected in the manual. It should correlate with the machine FCO log if all the FCOs have also been installed in the machine.

OPERATION

SECTION 2

INTRODUCTION

This section provides the information and instructions necessary for operating the drive and is divided into the following areas:

- Controls and Indicators - Locates and describes various controls and indicators related to operation of the drive.
- Operating Instructions - Describes procedures for operating the drive.

CONTROLS AND INDICATORS

GENERAL

The drive has two basic types of operator controls and indicators. These are (1) operator control panel (2) power supply control panel. These are shown on figure 2-1 and explained in the following.

NOTE

Additional controls and indicators contained on cards in the logic chassis and used primarily for maintenance are described in the hardware maintenance manual.

OPERATOR CONTROL PANEL

The operator control panel contains switches and indicators to control and monitor the basic operation of the drive. Figure 2-1 shows these controls and indicators and table 2-1 explains their functions.

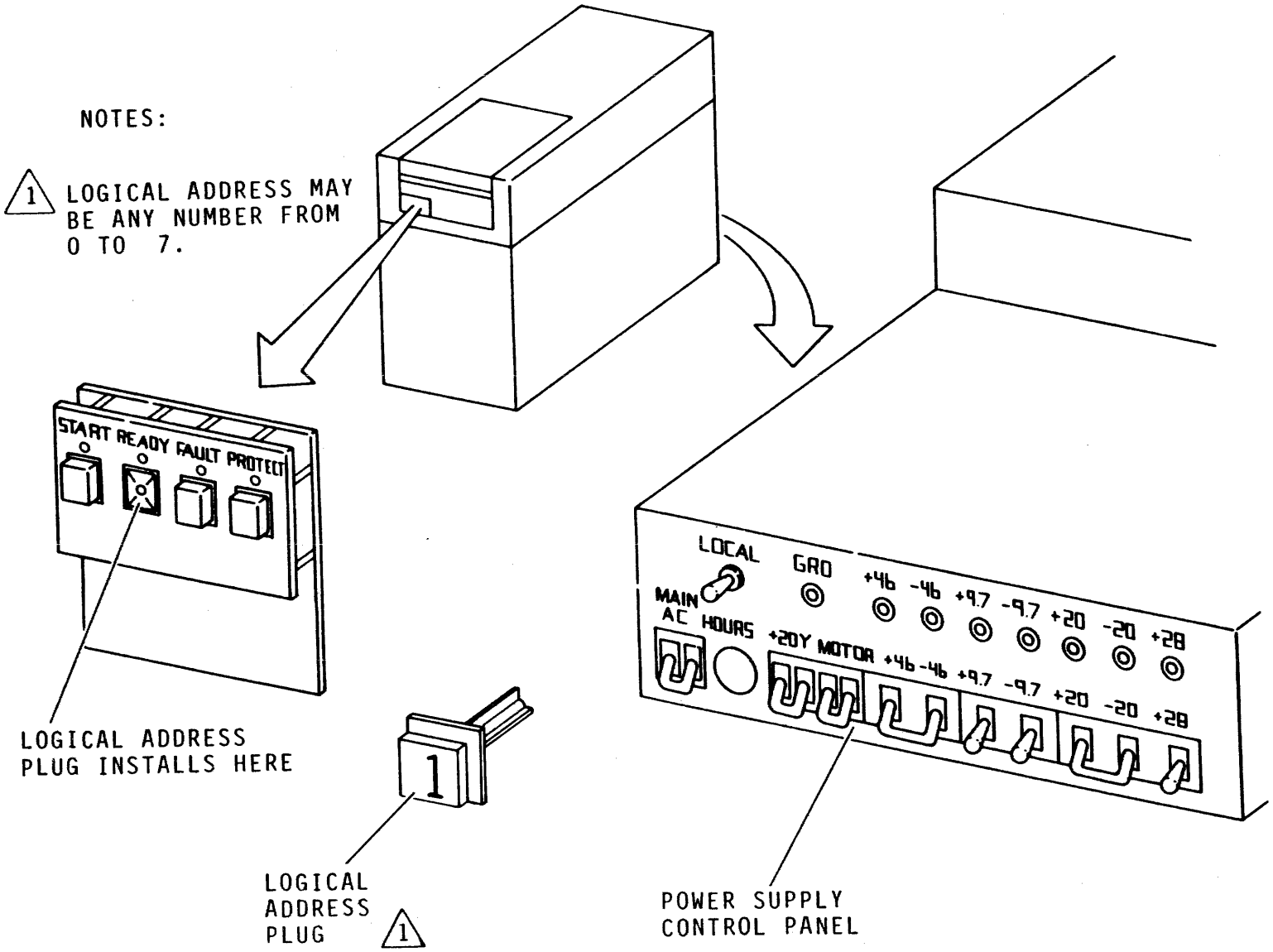


Figure 2-1. Controls and Indicators

TABLE 2-1. OPERATOR CONTROL PANEL FUNCTIONS

Control or Indicator	Function
Logical Address Plug	Determine logical address of drive. Address can be set any number from 0 to 7 by installing the proper plug. If no plug is installed the address is 7. Drive comes from the factory with complete set of logical address plugs each having a unique address. The available plugs with their associated address and part number are listed in the parts data section of the hardware maintenance manual.
START Switch/Indicator	Pressing button when drive is in power off condition (disk pack not spinning) lights indicator and starts power on sequence, provided the following conditions are met. • Disk pack is installed. • Pack access cover is closed. • All power supply circuit breakers are on. Pressing the indicator when drive is in power on condition (disk pack spinning), extinguishes indicator and starts power off sequence.
READY Indicator	Lights when unit is up to speed, the heads are loaded and no fault condition exists.
FAULT Switch/Indicator	Lights if a fault condition exists within the drive. It is extinguished by any of the following providing reason for fault is no longer present: • Pressing FAULT switch on operator control panel

Table Continued on Next Page

TABLE 2-1. OPERATOR CONTROL PANEL FUNCTIONS (Contd)

Control or Indicator	Function
WRITE PROTECT Switch/Indicator	• Fault Clear signal from controller • Maintenance Fault Clear switch on fault card in logic chassis location A17. Conditions causing fault are described in the discussion on Fault Detection in section 3 of this manual. Pressing switch to light indicator disables the driver write circuits and prevents it from writing data on the pack. Pressing the switch to extinguish the indicator removes the disable from the write circuits.

POWER SUPPLY CONTROL PANEL

The power supply control panel contains circuit breakers, test points and a time meter. These provide the means of controlling and monitoring operation of the power supply. The control panel is accessed by opening the rear door of the drive cabinet. Figure 2-1 shows the power supply control panel and table 2-2 explains their functions.

OPERATING INSTRUCTIONS

GENERAL

This discussion describes the procedures that are performed during normal operation of the drive. These procedures are: disk pack storage, disk pack removal and installation, power on and off.

TABLE 2-2. POWER SUPPLY CONTROL PANEL FUNCTIONS

Control or Indicator	Function
MAIN AC Circuit breaker	Controls application of site AC power to drive. Closing this breaker applies power to blower and elapsed time meter.
HOURS Elapsed time meter	Records accumulated AC power on time. Meter starts when MAIN AC circuit breaker is closed.
LOCAL/REMOTE	Controls whether drive can be powered up from drive or controller (remote). In LOCAL position, drive power on sequence starts when START switch is pressed. In REMOTE position, drive power on sequence starts when START switch is pressed and sequence power ground is received from controller.
+20Y, MOTOR, +46, -46, +9.7, -9.7, +20, -20, +28	Controls application of associated voltages to drive and also provides overload protection.

DISK PACK STORAGE

To ensure maximum disk pack life and reliability, observe the following precautions:

- Store disk packs in machine-room atmosphere (60°F to 90°F, 10% to 80% relative humidity).
- If disk pack must be stored in different environment, allow two hours for adjustment to computer environment before use.

- Never store disk pack in direct sunlight or in dirty environment.
- Store disk packs flat, not on edge. They may be stacked with similar packs when stored.
- Always be sure that both top and bottom plastic covers are on disk pack and locked together whenever it is not actually installed in a drive.
- When marking packs, use pen or felt tip marker that does not produce loose residue. Never use a lead pencil.
- Do not attach any label to the disk pack itself. Labels will not remain attached when the pack is spinning and catastrophic head crashes may result. All labels should be placed on the pack cannister if required.
- Cleaning of pack surfaces is not recommended.

DISK PACK HANDLING (CE AND DATA PACKS)

The positive pressure filtration system of the drive eliminates the need for periodic inspection and cleaning of the disk pack (media). However, should improper operating conditions of the pack be indicated by any of the following symptoms, immediately remove the pack from the drive.

1. A sudden increase in error rates related to one or more heads is observed.
2. An unusual noise such as pinging or scratching is heard.
3. A burning odor is smelled.
4. Contamination of the pack from dust, smoke, oil or the like is suspected.

If any doubt about the pack's functional condition exists, return it to the vendor, enclosing a description of the known or suspected malfunction.

CAUTION

Do not attempt to operate the media on another drive until full assurance is made that no damage or contamination has occurred to the media.

Do not attempt to operate the drive with another media until full assurance is made that no damage or contamination has occurred to the drive heads or to the shroud area.

DISK PACK INSPECTION AND CLEANING

In some cases, the user may attempt to inspect and clean the disk pack rather than return it to the vendor. This task must be performed by properly trained personnel only, using the following procedure.

NOTE

Inspection and cleaning of disk packs in the field can cause additional problems for the following reasons:

- Exposure of the pack to non-cleanroom conditions during inspection and cleaning may additionally contaminate the pack.
- Disk surfaces may be scratched by using contaminated or improper cleaning equipment.
- The pack may be damaged while the covers are removed.
- Deposits of cleaning solution residue may be left on disk surface if improperly cleaned or if commercial grade solutions are used.

CAUTION

Disk pack cleaning should never be attempted with the pack mounted on the drive, since this setup can introduce contamination into the drive itself.

1. Mount the pack on a commercially available pack inspection fixture.

2. Dampen, but do not soak, a lint-free swab-paddle with media cleaning solution (refer to the list of Maintenance Tools and Materials), or with a solution of 91% reagent grade isopropyl alcohol and 9% deionized water by volume.

3. Using a sweeping motion, insert the damp swab-paddle between the disks and manually rotate the pack while applying the swab-paddle lightly to the disk surface to be cleaned.

4. After the swab-paddle has been applied for one full cleaning rotation, withdraw it with a sweeping motion while maintaining contact with the disk surface (do not lift the swab-paddle from the surface.

5. If oxide or contaminants are observed on the swab-paddle, repeat steps 2, 3, and 4, using a clean swab-paddle for each pass, until no oxide or contaminants are observed on the swab-paddle.

6. Repeat steps 3 and 4 using a dry swab-paddle to remove all cleaning solution residue.

7. Repeat steps 2 through 6 for each surface.

DISK PACK INSTALLATION

The disk pack must be installed prior to performing any drive operations. Disk pack installation consists of setting the pack on the drive spindle and rotating the pack until the pack lockscrew is locked to the spindle lockshaft. The following describes this procedure.

CAUTION

Make certain that no dust or other foreign particles are present in shroud area. Also, ensure that blowers operate for at least two minutes prior to disk pack installation in order to purge blower system.

1. Set circuit breakers to on and observe that blower starts.

2. Raise pack access cover.

3. Disengage bottom dust cover from disk pack by squeezing levers of release mechanism in center of bottom dust cover and set cover aside to an uncontaminated storage area.

CAUTION

Non-fully retracted heads indicate a problem in the drives servo and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

NOTE

Top dust cover actuates parking brake when pack is set on spindle. Actuating brake holds spindle stationary while pack is installed. A click is heard as brake engages.

4. Set disk pack on spindle, avoiding abusive contact between disk pack and spindle, then twist clockwise until it is secured to spindle lockshaft.

5. Lift top dust cover clear of drive and store it with bottom dust cover.

CAUTION

Spin pack to ensure that removing top dust cover released parking brake.

6. Close pack access cover immediately to prevent entry of dust and contamination of disk surfaces.

DISK PACK REMOVAL

Disk pack removal consists of removing the pack from the spindle, installing the dust covers and setting the pack aside in an uncontaminated storage area. The following describes this procedure.

1. Press START switch to stop drive motor and unload heads.

2. When disk pack rotation has stopped completely, open pack access cover.

CAUTION

Non-fully retracted heads indicate a problem in the drives servo, and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

3. Place top dust cover over disk pack so post protruding from center of disk pack is received into dust cover handle.

4. Turn cover counterclockwise until disk pack is free of spindle.

CAUTION

Avoid abusive contact between disk pack and spindle.

5. Lift top cover and disk pack clear of drive and close pack access cover.

6. Place bottom dust cover on disk pack and store pack in an uncontaminated storage area.

POWER ON PROCEDURE

The following procedure describes how power is applied to the drive.

1. Set all power supply circuit breakers to on, and observe that blowers start.

CAUTION

Allow blowers to operate for at least two minutes before installing disk pack.

2. Install disk pack as instructed in disk pack installation procedure.

3. Set LOCAL/REMOTE switch to desired position.

4. Press START switch to light START indicator. If drive is in local mode, drive motor starts immediately and heads will load when motor is up to speed. If drive is in remote mode, drive motor starts and heads load whenever sequence power ground is available from controller (refer to discussion on power system in section 3 of this manual).

5. Observe that READY indicator lights when heads have loaded. The drive is now ready for online operations.

POWER OFF PROCEDURE

The power off sequence can be started either locally or remotely depending on the setting of the LOCAL/REMOTE switch. If this switch is in LOCAL, the sequence starts when the START switch is pressed to extinguish the START indicator. If the switch is in REMOTE, the sequence starts either when the START switch is pressed or when the sequence power ground signal is disabled at the controller (refer to discussion on Power System in section 3 of this manual).

In either case, the power off sequence unloads the heads, stops the drive motor and extinguishes the READY indicator.

THEORY OF OPERATION

SECTION 3

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. It is divided into the following major areas (refer to figure 3-1):

- Power System Functions - Describes how the drive provides the voltage necessary for drive operation.
- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the drives disk pack rotation, head positioning and air flow systems.
- Interface Functions - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.
- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.
- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disk pack.
- Machine Clock Functions - Explains how this circuit uses signals derived from the disk pack to generate timing pulses for the index, sector and read/write circuits.
- Sector Detection - Explains how the drive derives the sector pulses, which are used to determine the angular position with respect to Index of the read/write heads.

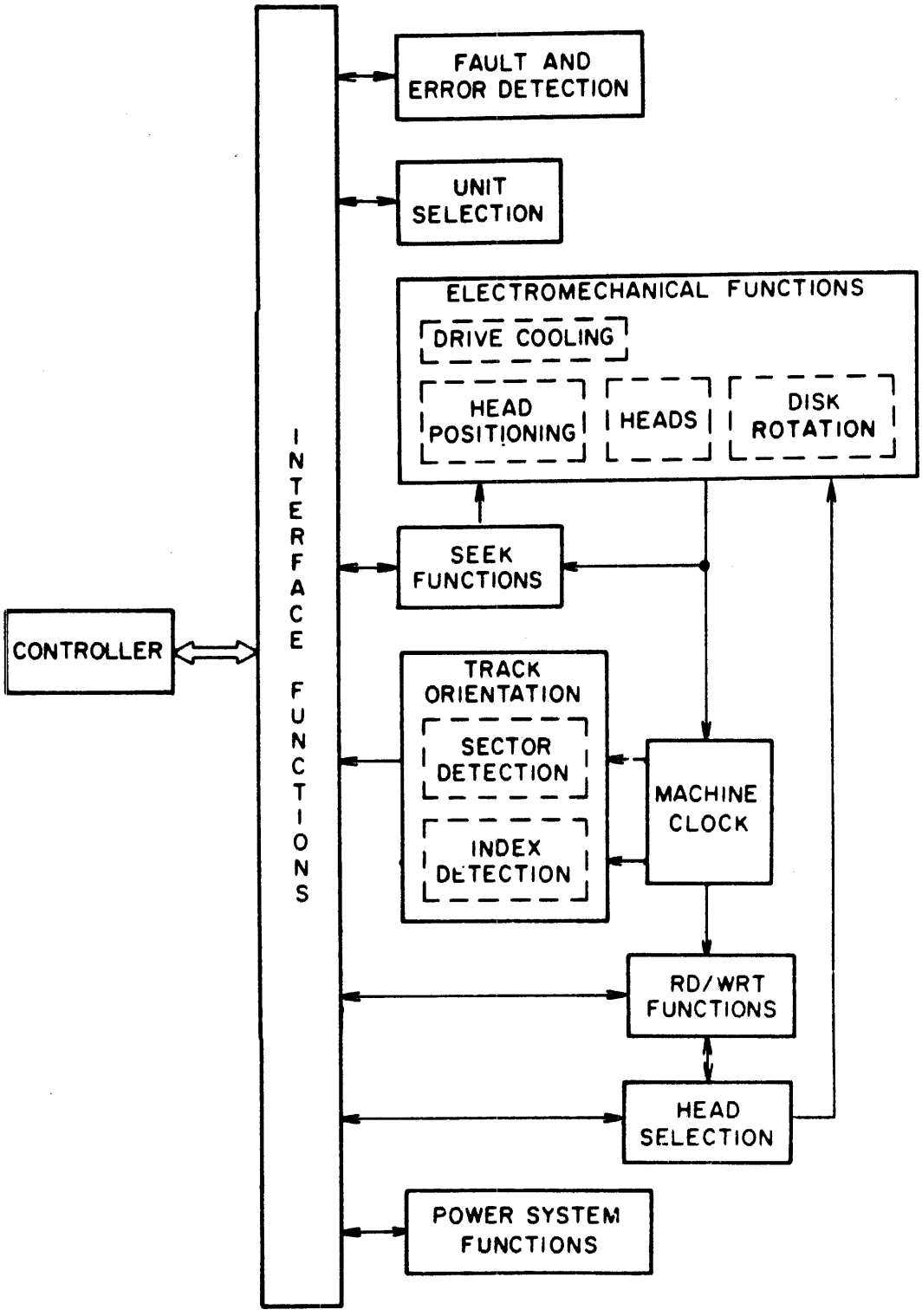


Figure 3-1. Drive Functional Block Diagram

- Head Selection - Explains the head selection process.

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk pack.

- Fault Detection - Describes the conditions that the drive interprets as faults.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in the hardware maintenance manual should take precedence over those in this manual if there is a conflict between the two.

POWER SYSTEM FUNCTIONS

GENERAL

The major element in the drives power system is the power supply. The power supply receives its input from the site ac power source and uses it to produce all the ac and dc voltages necessary for drive operation. These voltages are distributed to the drive circuitry via circuit breakers.

The drive motor is started and heads load function initiated during the power on sequence. The power off sequence unloads the heads and stops the drive motor. The drives LOCAL/REMOTE switch permits these sequences to be initiated either at the drive (local) or at the controller (remote).

The remainder of this discussion provides further description of the power system and is divided into the following areas:

- Power Distribution - Describes how the power is distributed to the drive circuitry.

- Local/Remote Power Sequencing - Explains how the drive may be powered up either at the drive or the controller.

- Power On Sequence - Describes how power is applied to the drive motor and the heads load sequence initiated.
- Power Off Sequence - Describes how the heads are unloaded and the drive motor stopped.
- Emergency Retract - Explains sequence performed when conditions exist requiring the heads be unloaded immediately to avoid damage to them or the disk pack.

POWER DISTRIBUTION

Power distribution consists of routing power to the various elements in the power supply and rest of the drive so that the power on sequence can be performed. The distribution is controlled by circuit breakers located within the power supply. These circuit breakers also provide overload protection for their associated voltages. The power distribution circuits are shown on figure 3-2 and basic operation is explained in the following.

Site main ac power is input to the power supply via the MAIN AC circuit breaker. When this breaker is closed, it applies power to the HOUR meter. It also provides the input to the drive motor control triacs; however, the motor does not start until the power on sequence.

Closing CB2 applies power to T3 and enables +20Y. With +20Y available, the transformers control triacs are enabled and power is applied to transformers T1 and T2 and the blower motor. These transformers provide inputs to the rectifier and capacitor board (-YEN), which in turn produces the dc voltages. The dc voltages are applied to the rest of the drive when their associated circuit breakers are closed.

When all circuit breakers are closed, the drives power on sequence can begin.

LOCAL/REMOTE POWER SEQUENCING CONTROL

General

The power on and off sequence of each drive can be controlled either locally or remotely depending on the setting of it LOCAL/REMOTE switch. When this switch is set to LOCAL, the sequences are initiated at the drive. When the switch is set to REMOTE, the sequences are initiated at the controller.

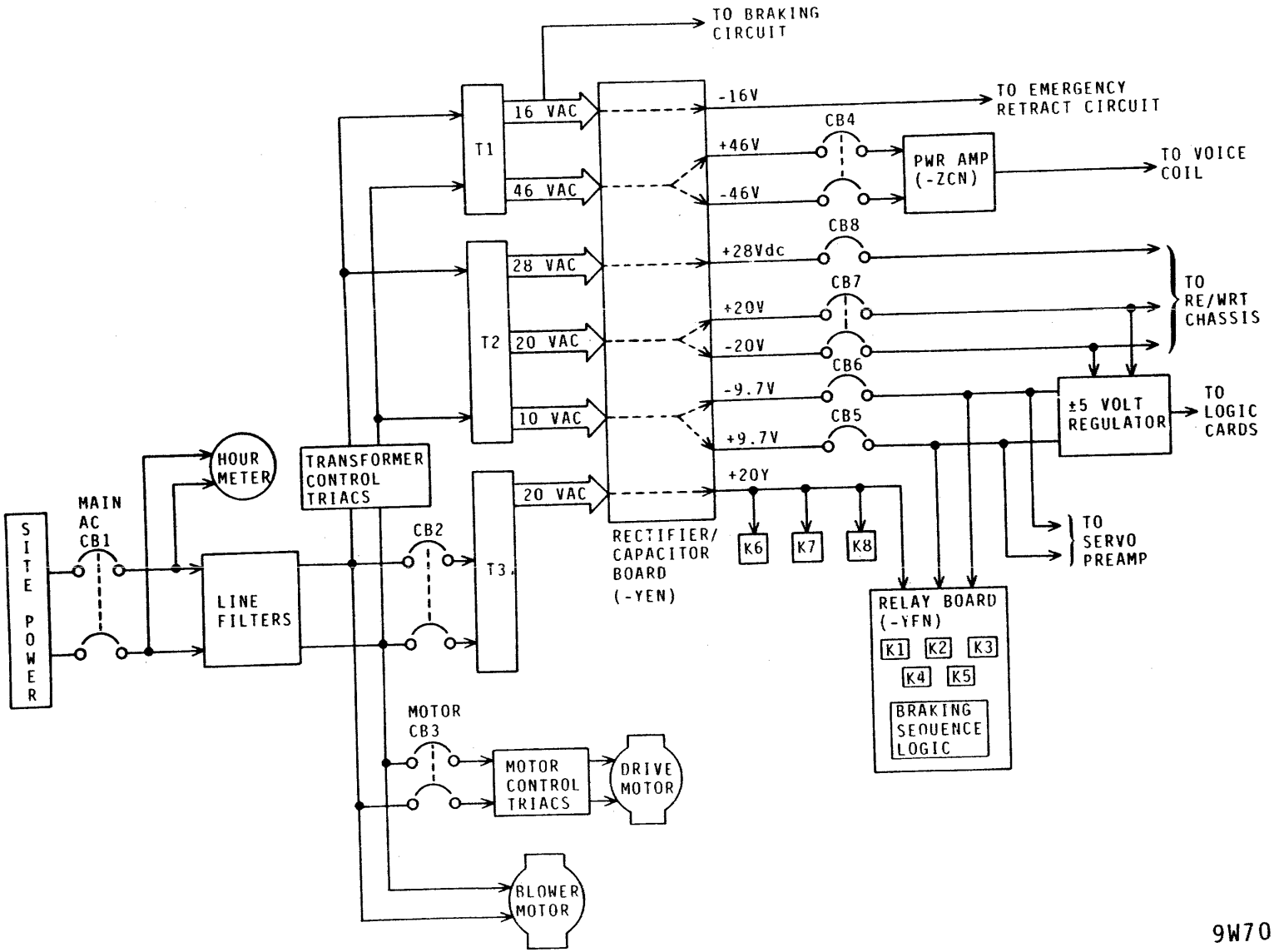


Figure 3-2. Power Distribution

The LOCAL/REMOTE switch is located on the power supply control panel and controls the mode of operation by determining how the drives sequence power relay (K1) is energized and de-energized. This relay works in conjunction with the drives START switch to control the power on and off sequences.

Figure 3-3 shows the LOCAL/REMOTE power sequencing control circuits. The operation of these circuits in both local and remote modes is explained in the following paragraphs.

Local Control

When the drive is in the local mode, the sequence power relay (K1) energizes whenever +20Y is available. This voltage is available whenever the MAIN AC circuit breaker (CB1) and +20Y circuit breaker (CB2) are closed. In this mode, the power on sequence begins when the START switch is pressed (providing all circuit breakers are closed). The power off sequence is initiated by pressing the START switch to extinguish the indicator.

Remote Control

If the drive is in the remote mode, the power sequence relay (K1) is energized by the power sequence signals (Pick and Hold) from the controller. The power on sequence does not begin unless these signals are received and the START switch is pressed. Both must occur for the power on sequence to take place.

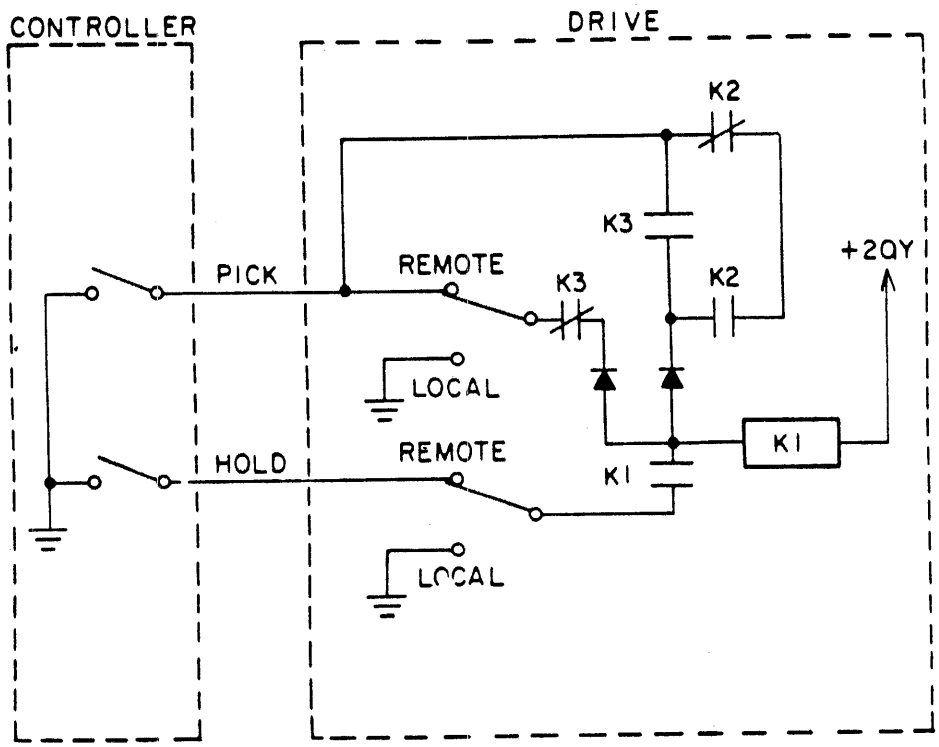
The drive is powered down either when the START switch is pressed or when the power sequence signals from the controller are deactivated.

Figure 3-4 is a flow chart of the remote power control sequence.

POWER ON SEQUENCE

The power on sequence starts the drive motor and initiates loading of the heads.

The sequence is initiated by pressing the START switch on the operator control panel. If all circuit breakers are closed, the disk pack is installed and the pack access cover is closed, pressing this switch energizes the Start relay (K2).



NOTE: 1. ALL RELAYS SHOWN IN THEIR NORMAL POWER OFF CONDITION.

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Figure 3-3. Local/Remote Power Sequencing Control Circuits

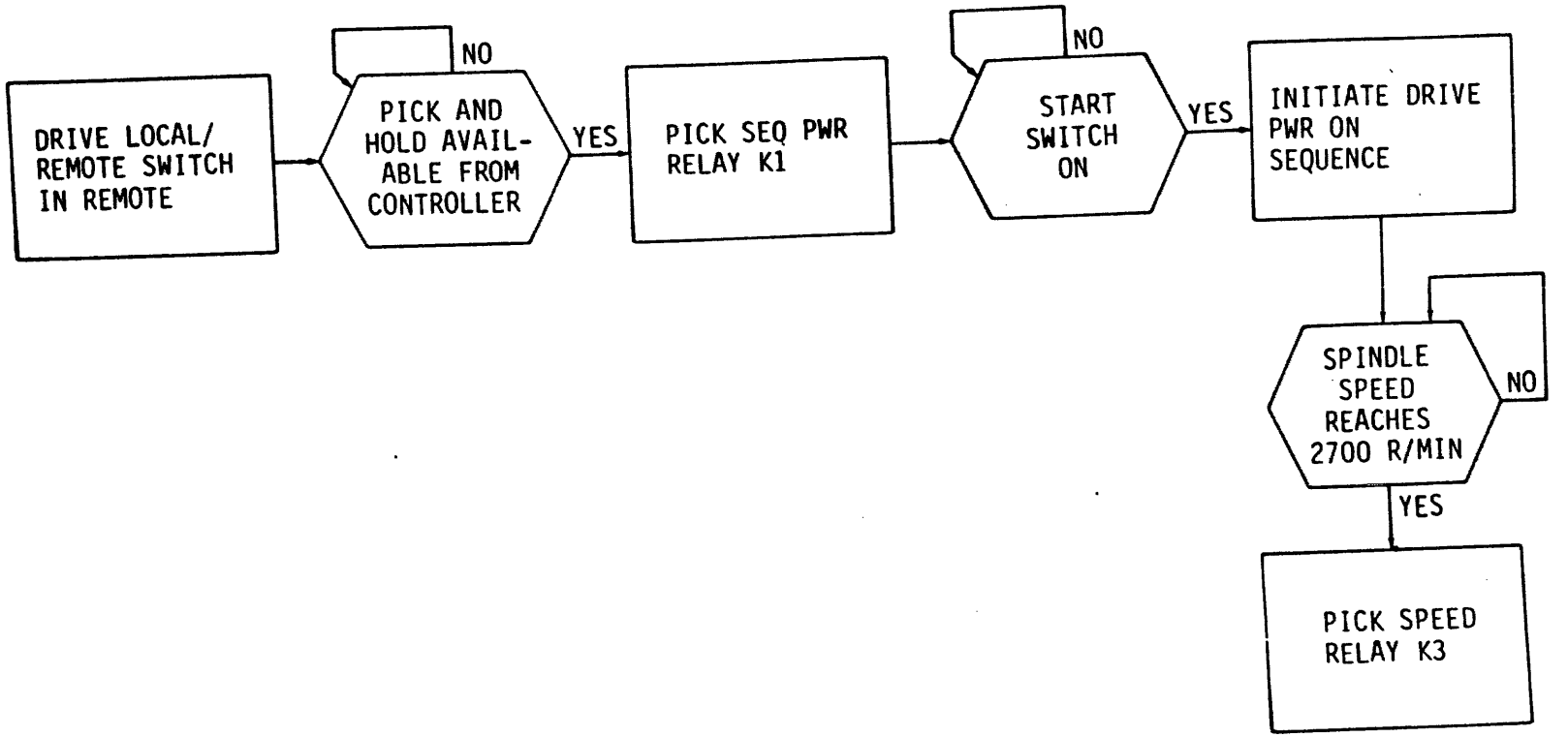


Figure 3-4. Remote Mode Power Sequencing

The Start relay causes the Motor relay (K4) to energize and enable the Motor Control triacs. This applies power to the drive motor causing it to start. The drive motor transfers motion to the spindle via the drive belt and the disk pack starts to rotate.

When the speed sensing circuits indicate the spindle speed is about 2700 r/min, the Speed relay (K3) energizes. This does two things (1) energizes the Emergency Retract relay (K7) and (2) triggers the 10 second Load Delay one shot.

Energizing the Emergency Retract relay connects the power amplifier to the voice coil and connects the Emergency Retract capacitor to -16 volts. This prepares the voice coil to respond to commands from the servo logic and charges the Emergency Retract capacitor so it is ready for an emergency retract condition.

The Heads Load Delay allows the spindle time to reach 3000 r/min before enabling the heads load logic. When the delay times out, the heads load sequence is initiated causing the heads to load. This sequence is covered in the discussion on Load Seeks.

Figure 3-5 shows the circuitry involved in the power up sequence and figure 3-6 is a flow chart of the operation.

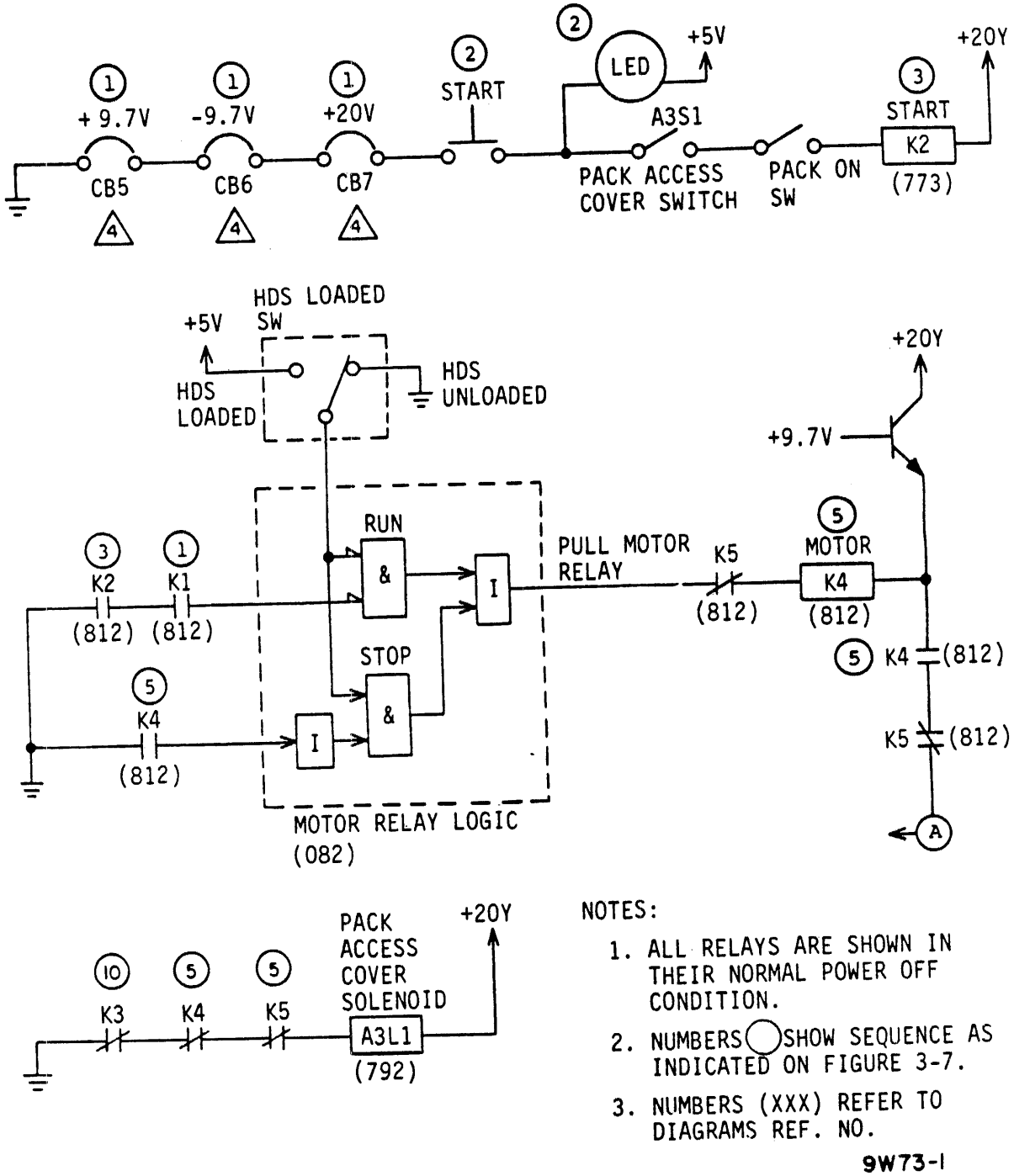


Figure 3-5. Power On Circuit (Sheet 1 of 2)

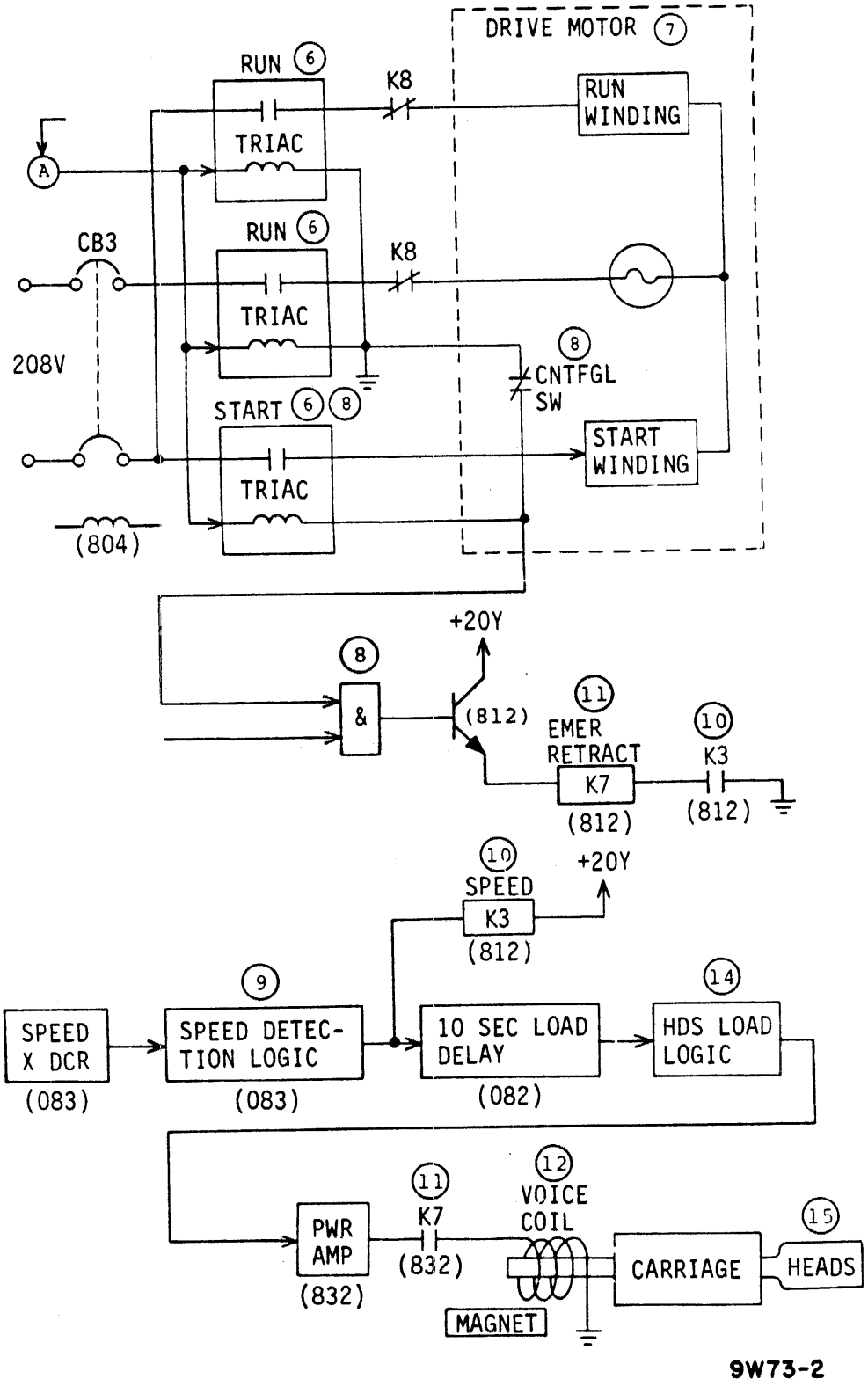


Figure 3-5. Power On Circuit (Sheet 2)

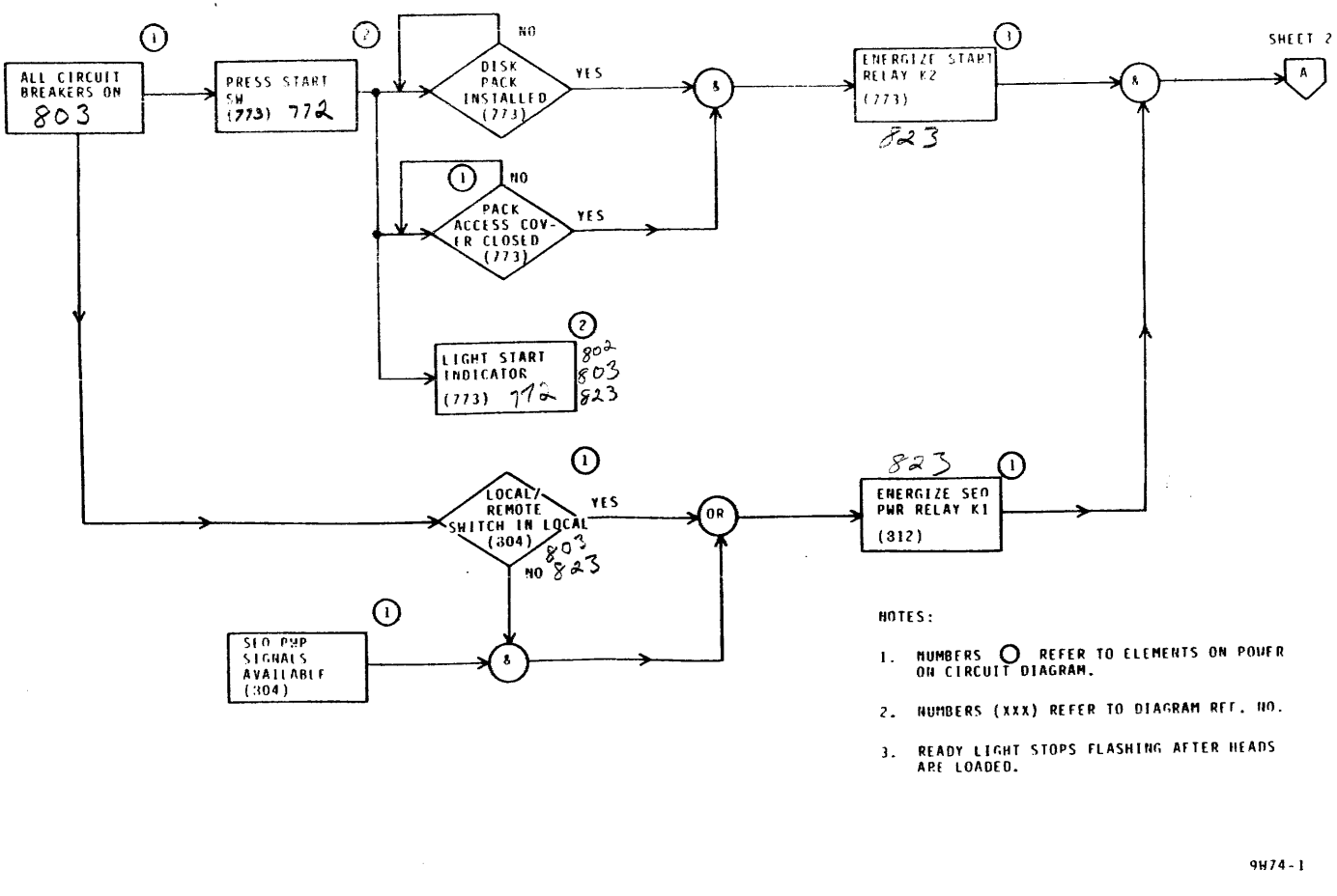


Figure 3-6. Power On Sequence Flow Chart (Sheet 1 of 2)

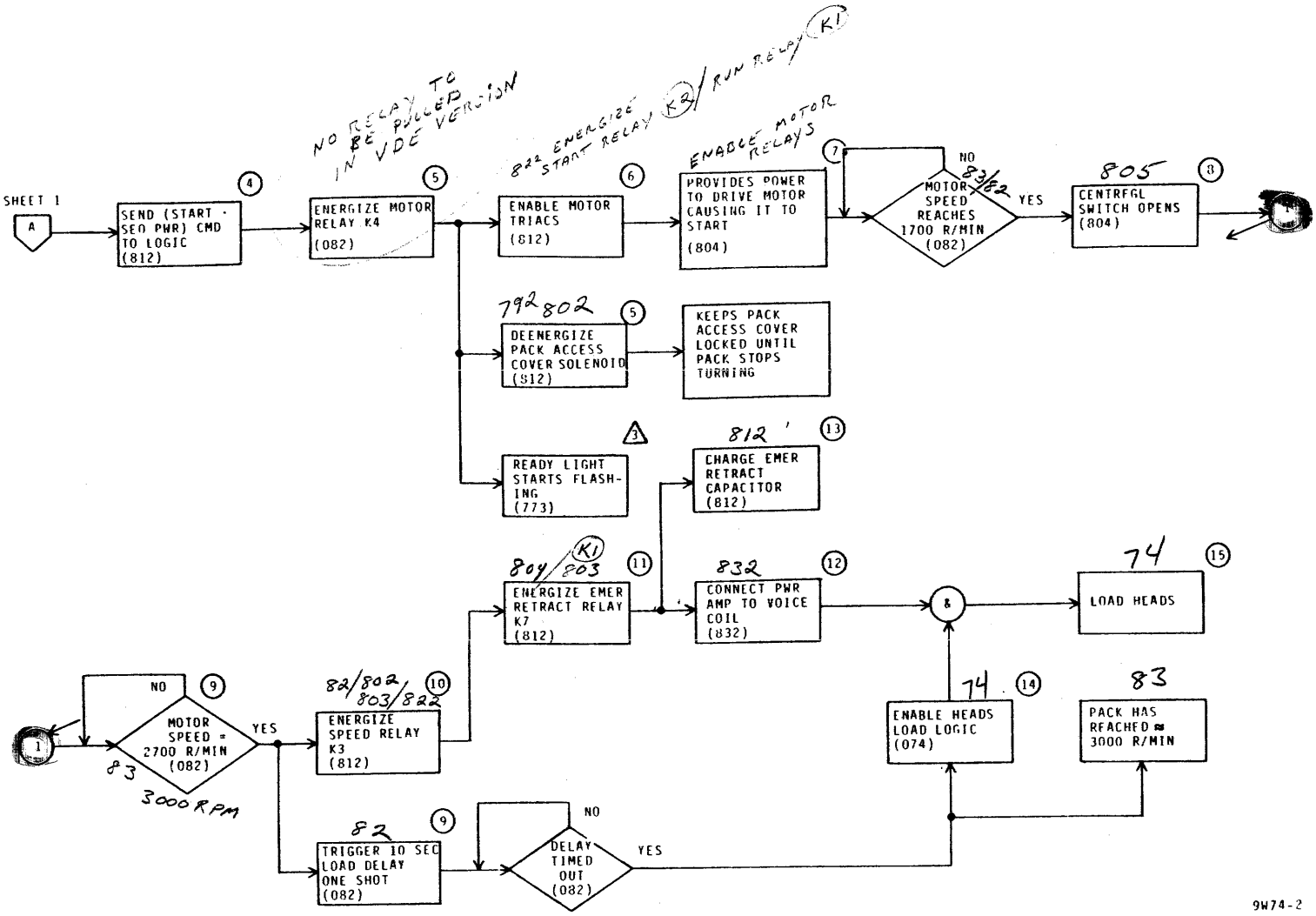


Figure 3-6. Power On Sequence Flow Chart (Sheet 2)

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive motor.

The sequence begins when either the START switch is pressed or the Sequence Power relay (K1) is deenergized. In either case the Start relay (K2) deenergizes and the RTZ logic is enabled (refer to discussion on Return to Zero Seeks). This causes the heads to move in the reverse direction.

When the heads unloaded switch indicates the heads are unloaded, the RTZ logic is disabled and the motor relay (K4) is deenergized. Deenergizing the Motor relay (K4) removes power from the drive motor and enables the braking logic. Enabling the brake logic initiates the braking sequence.

The braking sequence begins by energizing the Brake Power relay (K5) which in turn energizes the Brake relay (K8). The Brake relay applies -16 Vdc causes a current to flow through the winding and the magnetic field generated by this current has a braking effect on the motor.

The motor slows down and when its speed is less than 2700 r/min, the Speed relay (K3) deenergizes. This in turn causes the Emergency Retract relay (K7) to deenergize thus disconnecting the power amplifier from the voice coil.

The Brake power and Brake relays deenergize approximately 30 seconds after the start of the braking sequence. This removes braking voltage from the drive motor, which by this time is stopped. This also removes power from the pack access solenoid thus allowing the pack access cover to be opened.

Figure 3-7 shows the circuitry involved in the power off sequence and figure 3-8 is a flow chart of the operation.

EMERGENCY RETRACT

The emergency retract function provides an emergency means of retracting the heads from the pack area. This sequence is initiated if disk speed is reduced or if conditions indicate that it may be reduced. Failure to retract the heads under these conditions could result in head crash a subsequent damage to the heads and disk pack.

Any of the following conditions initiate an emergency retract sequence:

- Loss of AC Power - If site ac power is lost, all dc power is also lost. This power loss includes +20Y, +9.7, and -16 V, any of which cause an emergency retract to occur.

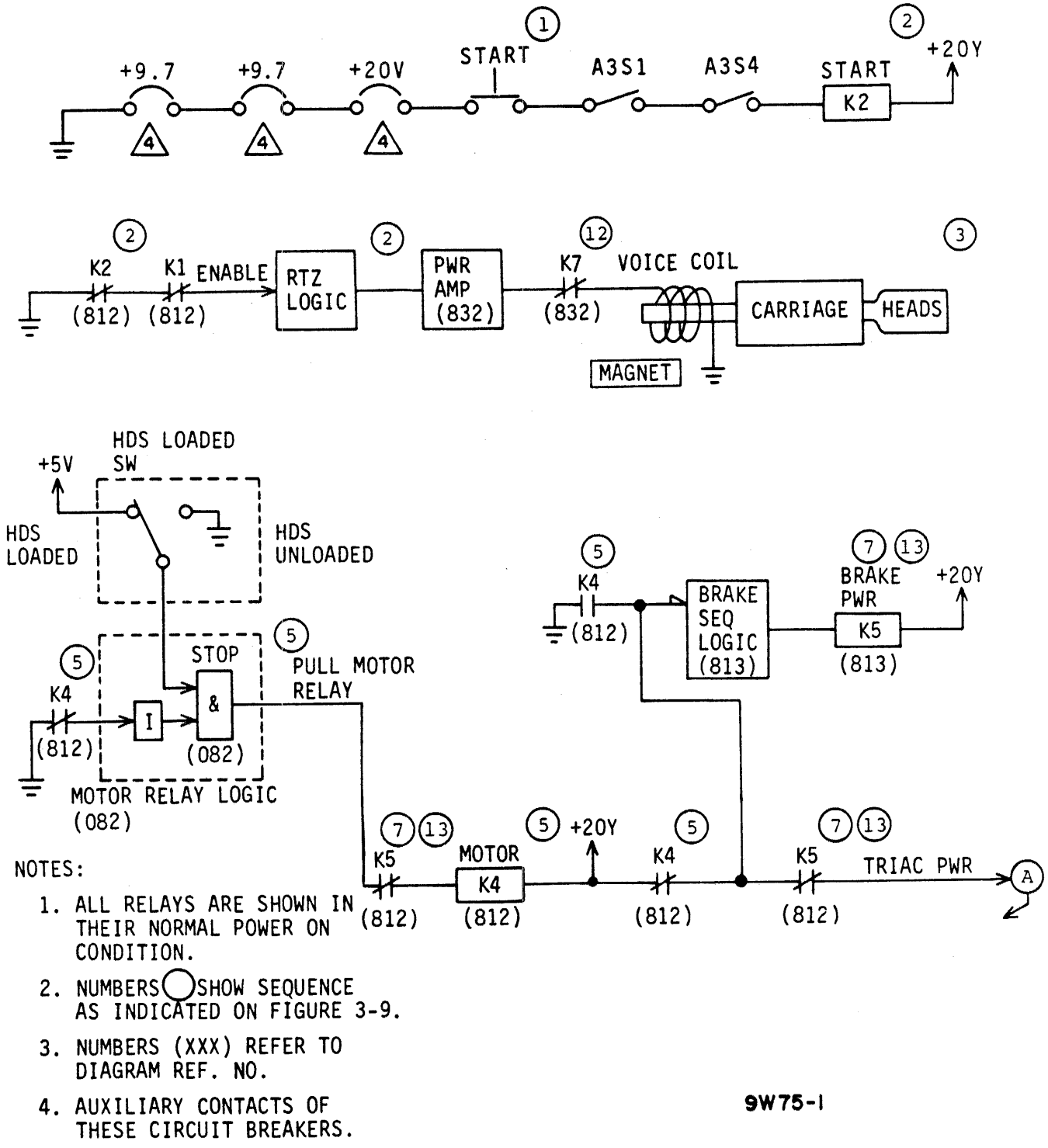


Figure 3-7. Power Off Circuits (Sheet 1 of 2)

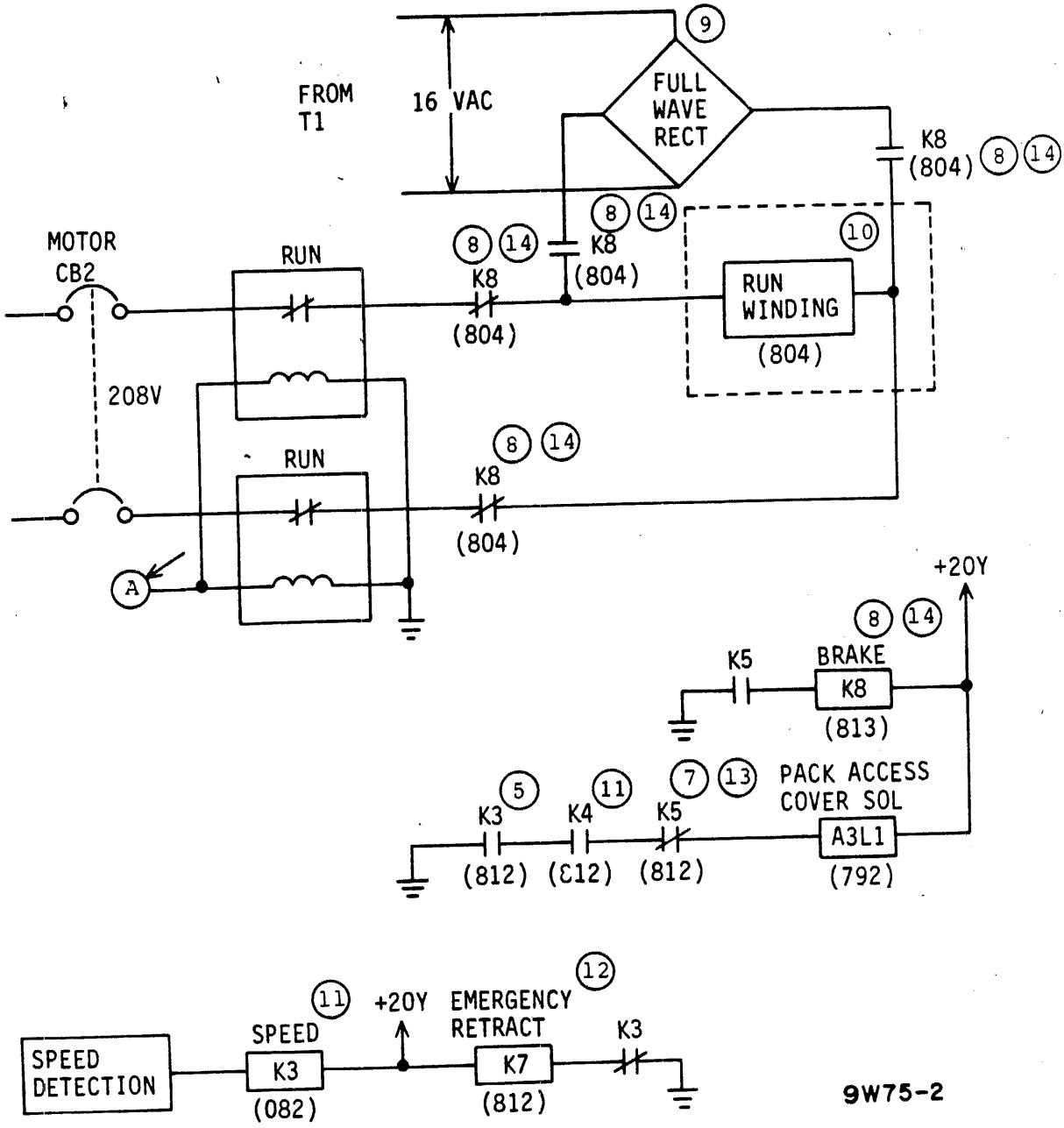


Figure 3-7. Power Off Circuits (Sheet 2)

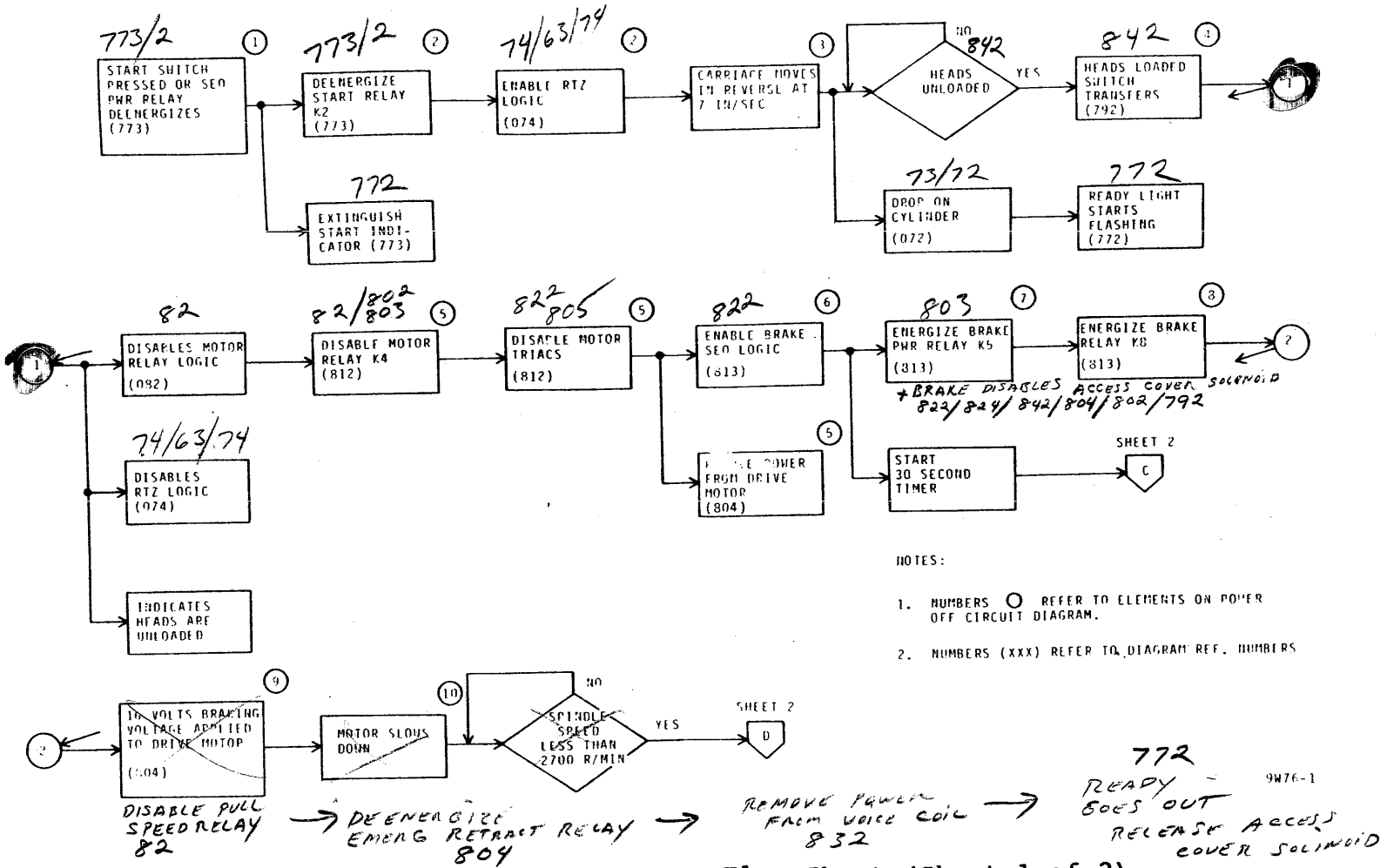


Figure 3-8. Power Off Sequence Flow Chart (Sheet 1 of 2)

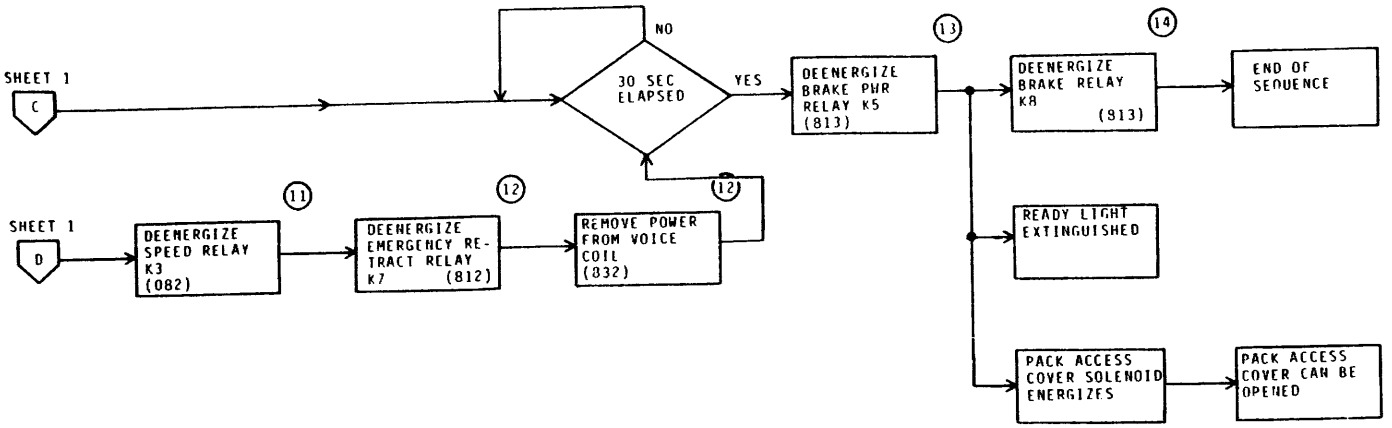


Figure 3-8. Power Off Sequence Flow Chart (Sheet 2)

- Loss of +20Y, -16, or +9.7 V - Losing any of these voltages directly causes the emergency retract relay to deenergize thus starting the emergency retract sequence.

- Loss of Speed - If spindle motor speed drops below 2700 r/min, the speed detection circuits cause the emergency retract capacitor to deenergize.

- Drive Motor Thermal Overload - If the drive motor overheats, a thermal relay within the motor opens. This results in the Motor circuit breaker opening and removing power from the drive motor. The motor then slows down and the loss of speed causes a emergency retract.

Figure 3-9 shows the circuitry involved in the emergency retract sequence.

ELECTROMECHANICAL FUNCTIONS

GENERAL

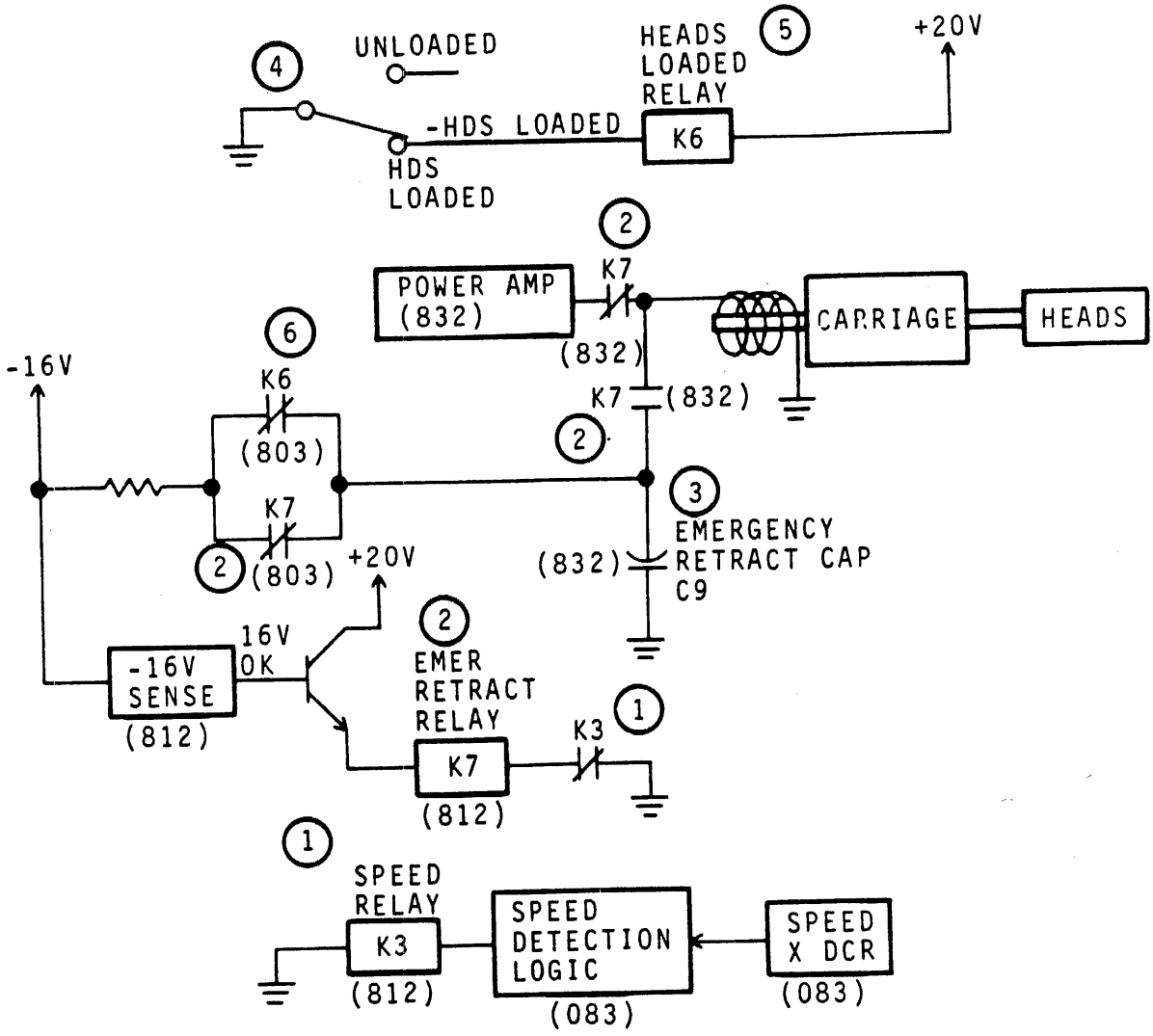
Certain drive functions are a result of the electromechanical devices working under the control of logical circuitry. These functions include disk pack rotation, head positioning, and drive cooling and ventilation..

Disk pack rotation is performed by the disk pack rotation mechanism, which is controlled by the power system. The purpose of disk pack rotation is to create a cushion of air on the disk surfaces. The cushion of air allows the heads (which read and write the data) to move over the disk surfaces without actually contacting them.

The heads are positioned over specific data tracks on the disk surface by the head positioning mechanism. The mechanism is controlled by the servo circuits (refer to discussion fo Seek Operations) and the power system.

Drive cooling and ventilation is provided by the air flow system. The main element in this sytem is the blower motor which receives its power from the power system.

Figure 3-10 is a block diagram showing each of the previously discussed mechanisms. A more detailed physical and functional description of each is provided in the following discussions.



NOTES:

1. ALL RELAYS ARE SHOWN IN ENERGIZED CONDITION.
2. NUMBERS ◯ REFER TO SEQUENCE OF EVENT DURING EMERGENCY RETRACT.
3. NUMBERS (XXX) REFER TO DIAGRAM REF. NO.

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Figure 3-9. Emergency Retract Circuits

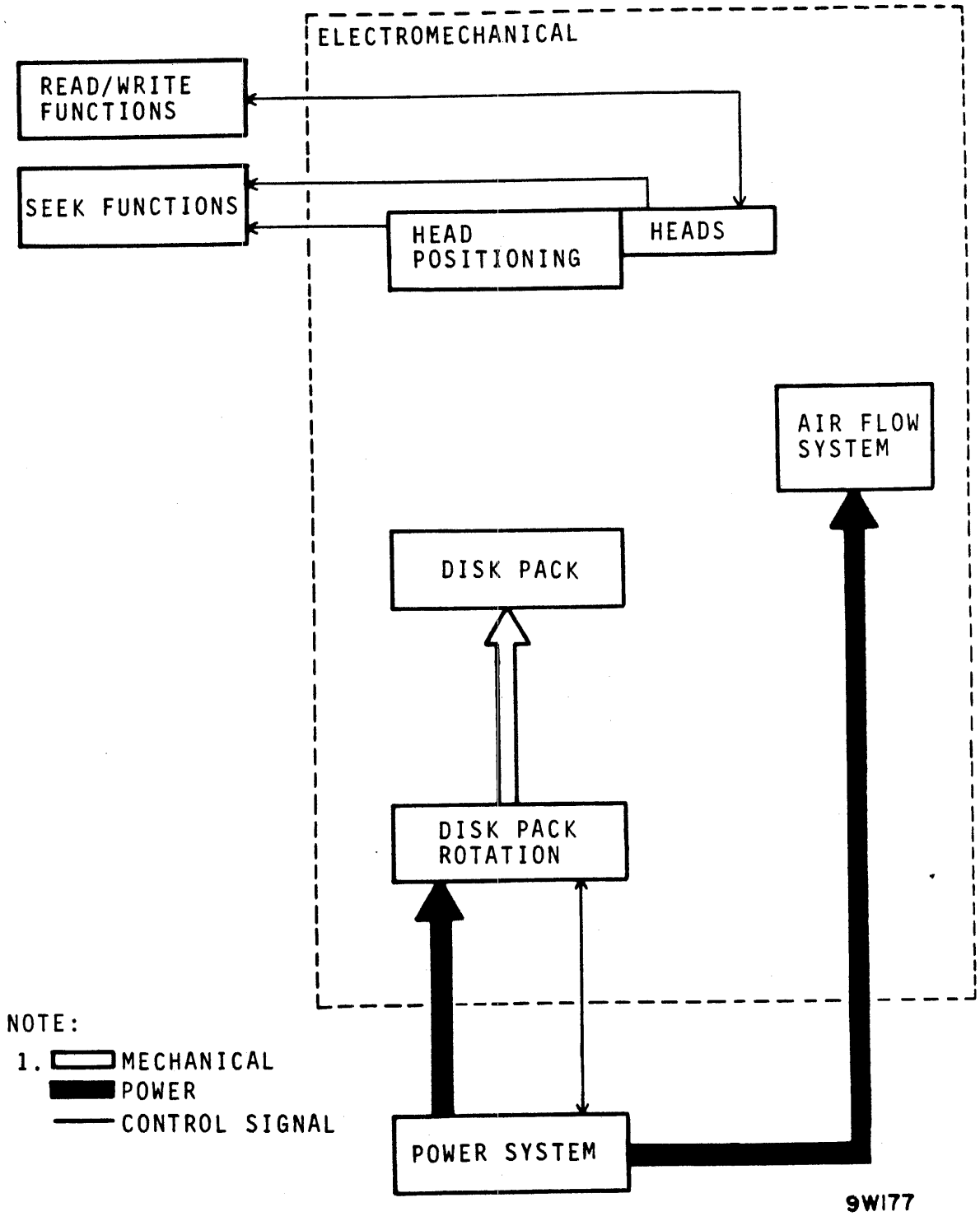

Figure 3-10. Electromechanical Functions Block Diagram

DISK PACK ROTATION

General

The disk pack must be rotating fast enough to allow the heads to fly before any drive operation can be performed. The following mechanisms work in conjunction with the power system to control disk pack rotation (refer to figure 3-11):

- Drive Motor - Provides rotating motion for the spindle and disk pack.
- Spindle - Provides rotating mounting surface for disk pack.
- Parking Brake - Holds spindle while pack is being installed.
- Speed Sensor - Generates pulses that are used to determine speed of spindle.
- Pack On Switch - Actuated when pack is installed on spindle, this device must indicate the pack is installed before the power on sequence can be performed.
- Pack Access Cover Switch - Ensures that pack access cover is closed before disk pack rotation begins.
- Pack Access Cover Solenoid - Prevents pack access cover from being opened while pack is rotating.

These mechanisms are further described in the following paragraphs.

Drive Motor

The drive motor provides the rotational energy required to rotate the spindle and disk pack. The motor is mounted on a movable plate which in turn is mounted on the underside of the deck casting (refer to figure 3-12).

Motion is transferred from motor to spindle via the drive belt. This belt connects the pulley on the shaft of the drive motor to the pulley on the lower end of the spindle.

The springs attached between the motor mounting plate and deck casting, maintain enough tension on the plate to keep the drive belt tight. The spring tension is adjustable so tension on the belt can be adjusted to provide the best coupling between drive motor and spindle pulleys.

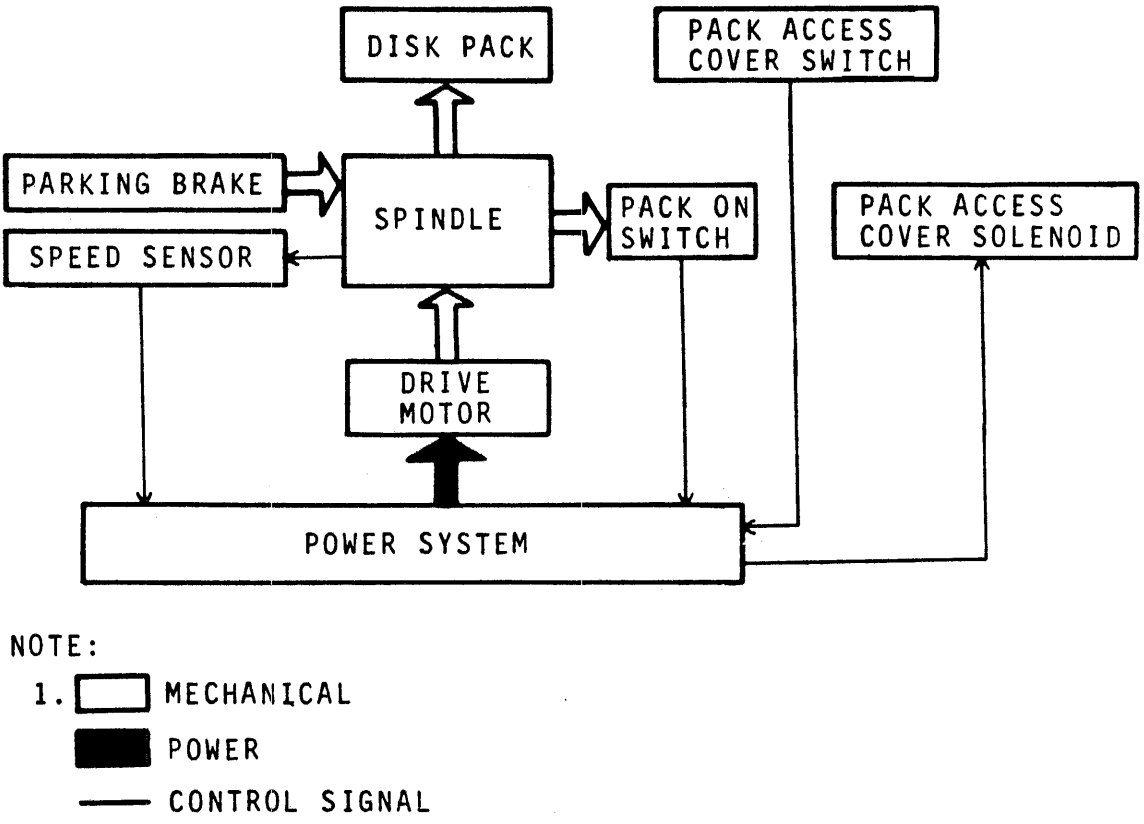

Figure 3-11. Disk Pack Rotation Functional Block Diagram

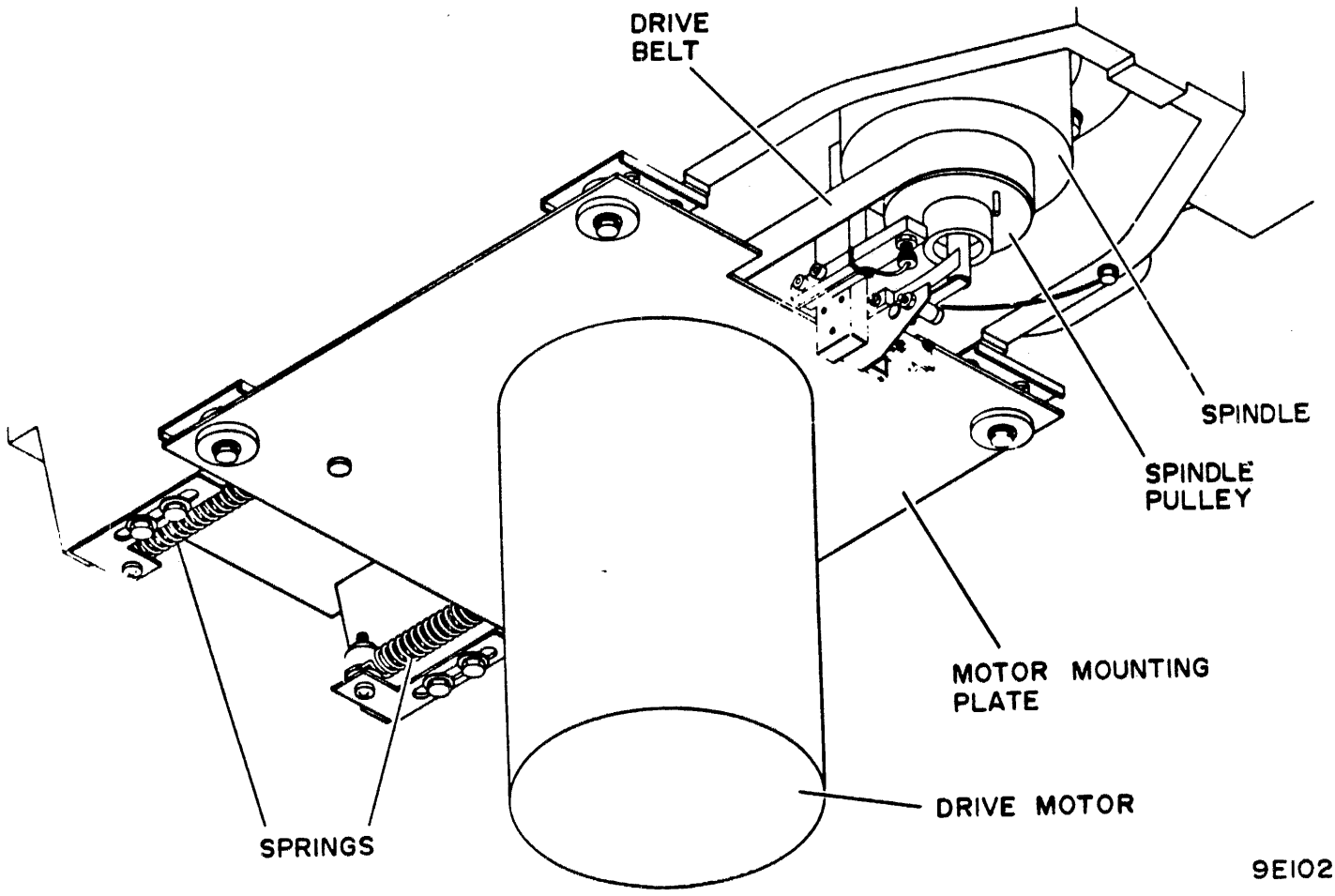

Figure 3-12. Drive Motor Assembly

The motor starts during the power on sequence when power is applied to its start and run windings (refer to Power On Sequence discussion). The start winding helps the run winding start the motor in motion and get it up to speed. When the motor speed reaches approximately 1700 r/min, the start winding is no longer needed and a centrifugal switch (within the motor) opens thus disabling the start winding. The motor continues to accelerate (using only its run winding) until it reaches its maximum speed (approximately 3600 r/min). This speed is maintained until power is removed from the motors run winding (refer to discussion on Power System).

The temperature of the motor is monitored by the thermal switch. If the motor overheats, this switch opens resulting in loss of power to the drive motor. The motor slows down causing an emergency retract and power off sequence. The drive motor cannot be restarted until it cools off, thereby causing the thermal switch to close.

Spindle

The spindle (refer to figures 3-13 and 3-14) provides the means of mounting the disk pack within the drive and also of rotating the pack when the drive motor is energized.

When the pack is mounted, its lower disk rests on the pack mounting plate. This plate connects to a shaft which in turn connects to the pulley on the lower end of the spindle. When the drive motor starts, it transfers motion to this pulley via the drive belt and causes the pack mounting plate and disk pack to rotate.

The disk pack must be secured to the mounting plate with enough force so the two of them will rotate together. This force is provided by the lockshaft, which is a spring loaded shaft located within the spindle. When the pack is installed, the mounting screw on the bottom of the pack is threaded into the internal threads in the upper end of the lockshaft. As the pack is tightened down against the mounting plate, the springs holding the lockshaft exert a downward force on the pack. When this force is sufficient, a release mechanism (in the handle of the disk pack top dust cover) releases the top dust over from the pack. The pack is now installed and will rotate whenever the drive motor is energized.

A ground spring (refer to figure 3-13) bleeds off any static electricity accumulating on the spindle.

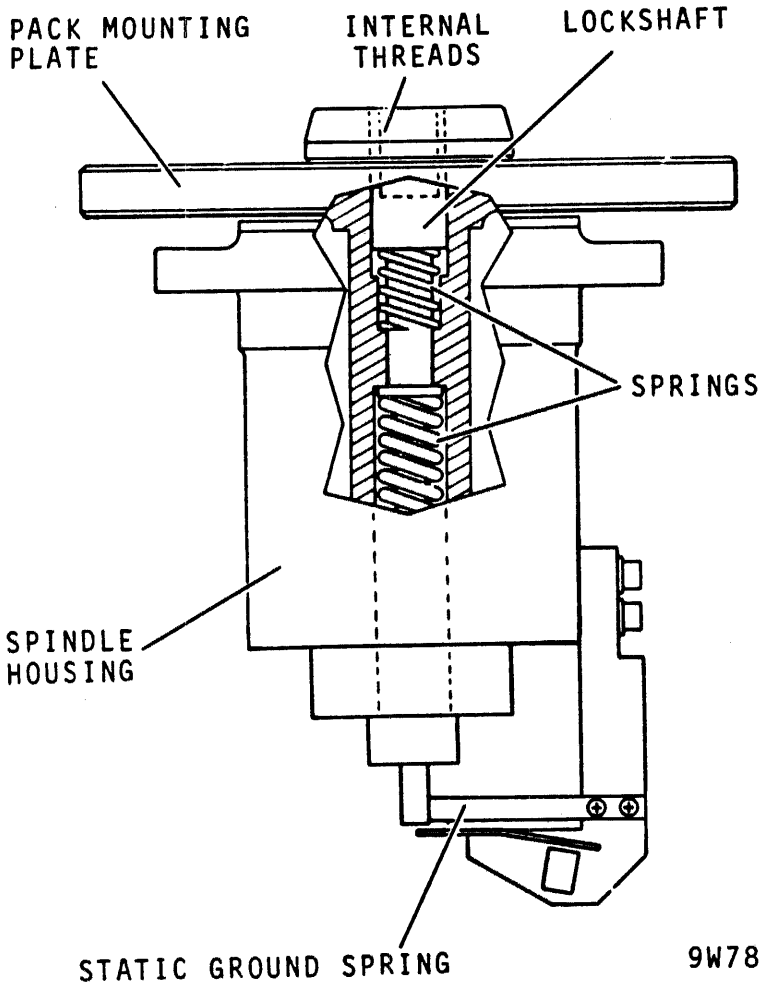

Figure 3-13. Spindle Assembly

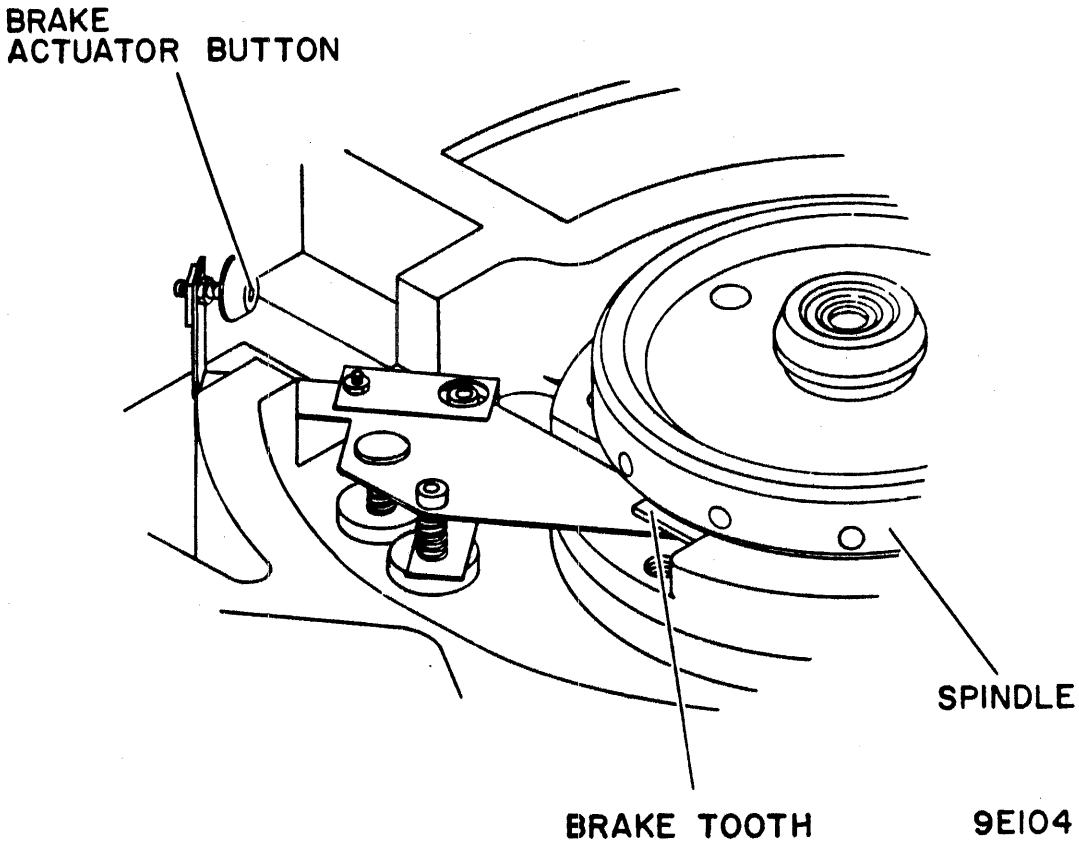

Figure 3-14. Parking Brake Assembly

Parking Brake

The parking brake (refer to figure 3-14) holds the spindle stationary whenever a disk pack is installed or removed. It is actuated by the disk pack top dust cover which contacts the brake actuator button. This causes the brake tooth to move up and engage a slot in the bottom of the spindle thus preventing the spindle from rotating. When the dust cover is removed, the actuator button is released, the brake tooth disengages, and the spindle is free to turn.

Speed Sensor

The speed sensor (refer to figures 3-15 and 3-16) is a device that generates signals used to determine if spindle speed is sufficient to allow the heads to fly. The sensor is mounted beneath the spindle and consists of a small coil and core assembly. The coil has a current flowing through it and each time the pin mounted on the bottom of the rotating spindle aligns itself with the core of the coil, a signal is generated.

The speed sensor logic monitors these signals and uses them to determine if spindle speed is at least 3000 r/min. When this speed is reached, the speed relay is energized; and it remains energized as long as this speed is maintained. However, if spindle speed drops below 3000 r/min the speed relay deenergizes refer to discussion on Emergency Retract).

Pack On Switch

The disk pack must be securely installed on the spindle for the drive motor to run. This condition is ensured by the pack on switch. The switch is located beneath the spindle (refer to figure 3-15) and is actuated by the lockshaft when the pack is installed.

If the pack is not completely installed, the switch will not be closed and the drive motor will not start. If the pack comes loose during drive operation and the pack on switch opens, the power off sequence is initiated thus stopping the drive motor.

Pack Access Cover Switch

In addition to the pack on switch, the pack access cover switch (refer to figure 3-16) must be closed for the drive motor to run. This switch ensures that the pack access cover is closed.

Opening the switch has the same effect as opening the pack on switch.

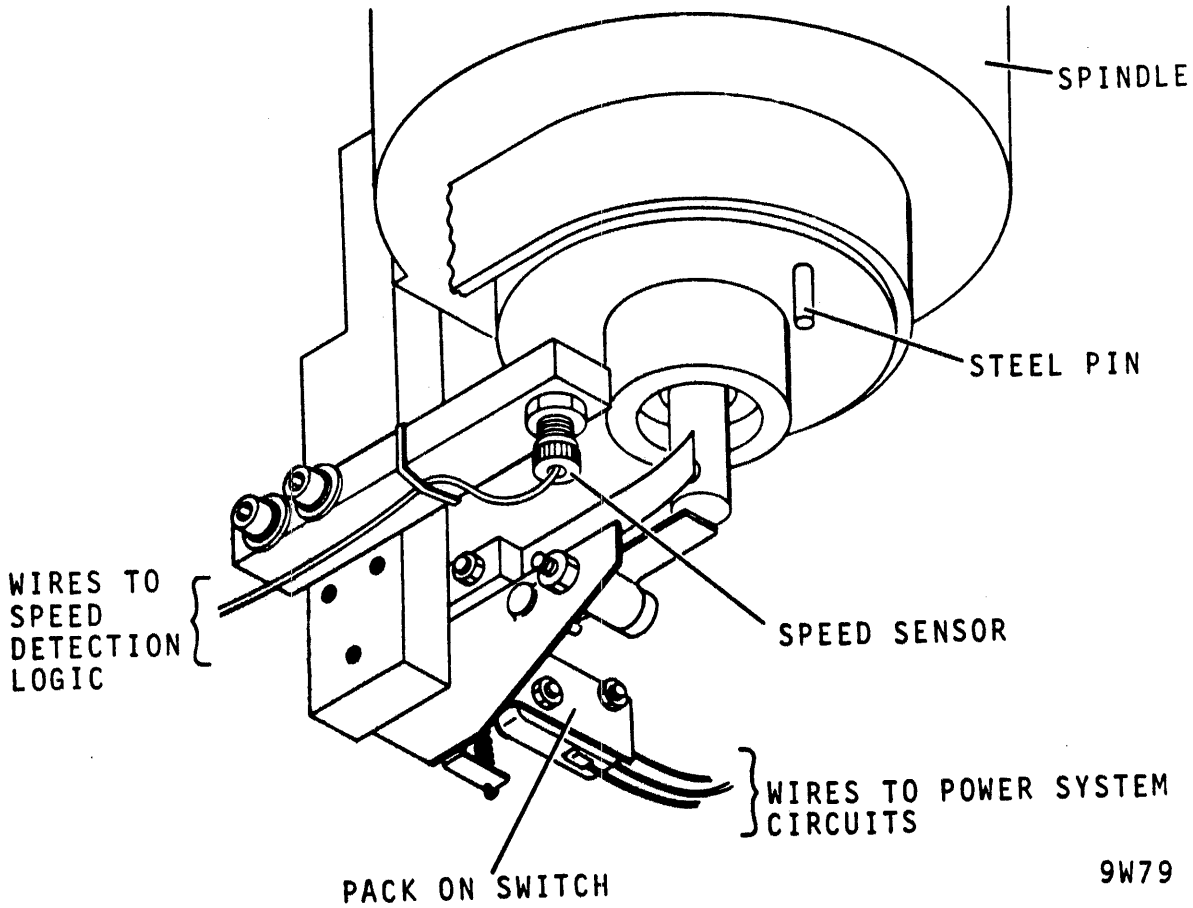

Figure 3-15. Speed Sensor and Park On Switch Assemblies

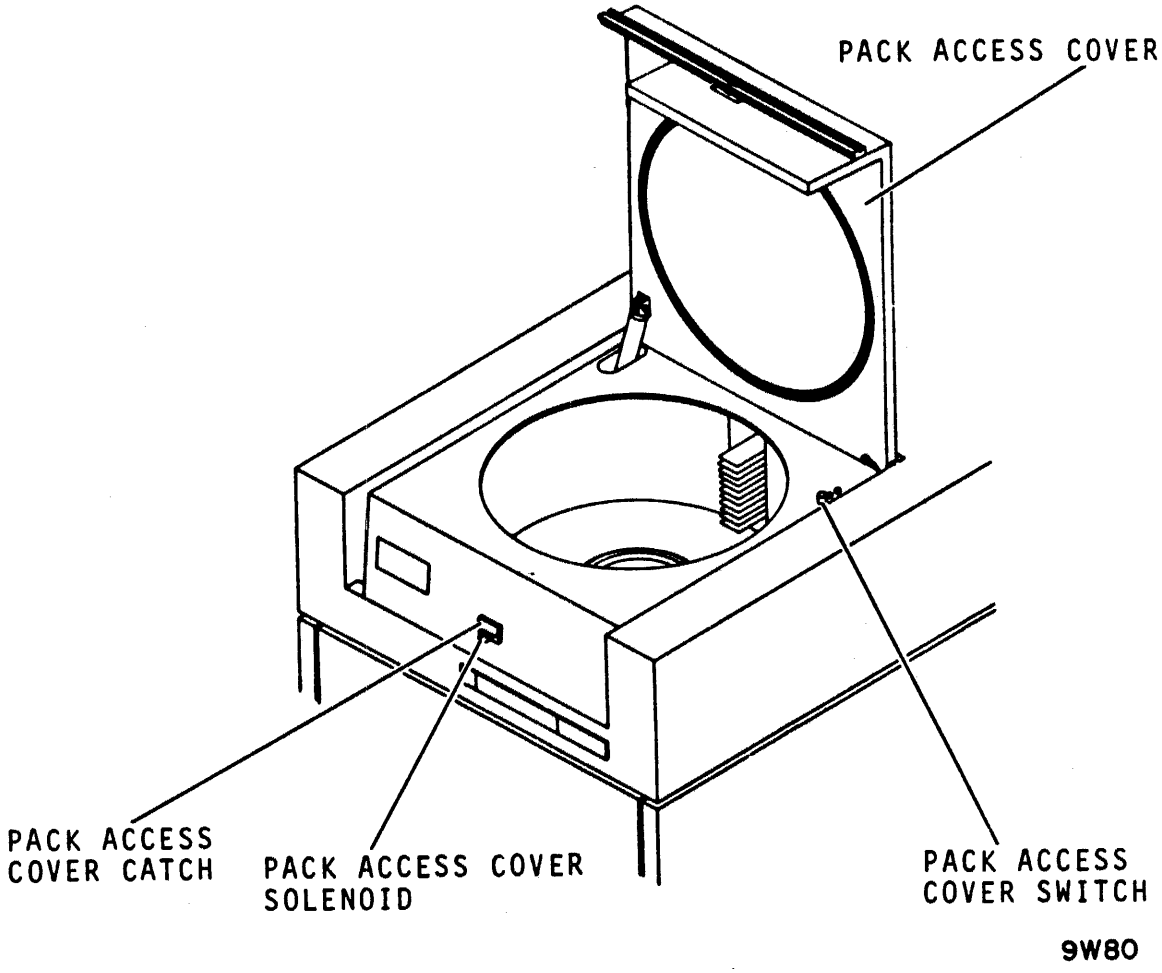

Figure 3-16. Pack Access Cover Switch and Solenoid

Pack Access Cover Solenoid

If the drive is equipped with a pack access cover solenoid (refer to figure 3-16), the pack access cover can be opened only if the drive is in the standby condition, that is with the circuit breakers on but the heads unloaded and the disk not rotating. The solenoid controls the operation of the pack access cover as follows.

During the power on sequence when the pack starts turning, the solenoid is deenergized and a spring pushes the solenoid arm upwards. This locks the pack access cover latch and prevents the cover from being opened.

If the drive is in the standby condition, the solenoid is energized and the arm is pulled down. This releases the pack access cover latch and allows the cover to be opened.

HEAD POSITIONING

General

Data is read from and written on the disk by the heads. However, the drive must position the heads over a specific data track on the disk before a read or write operation can be performed. Head positioning is performed by the head positioning mechanism.

This mechanism consists of the actuator, magnet, velocity transducer and heads loaded switch.

The actual positioning is performed by the actuator and magnet. The positioner is controlled by signals received from the servo circuits (refer to discussion on Seek Functions).

The velocity transducer and heads loaded switch provide signals that are used by the servo circuits in controlling head positioning.

Figure 3-17 is a functional block diagram of the head positioning mechanism. The following paragraphs provide further description of the elements shown on this figure.

Actuator and Magnet

General

The actuator and magnet (refer to figure 3-18) work in conjunction to position the heads. The following is a physical and functional description of the actuator and magnet assemblies.

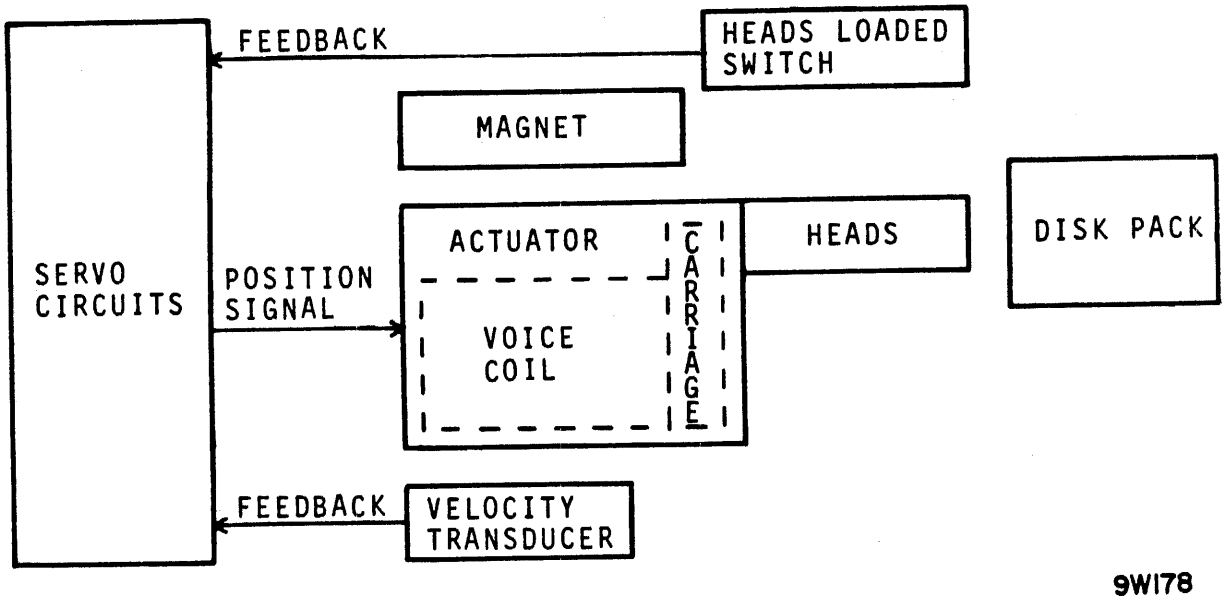

Figure 3-17. Head Positioning Functional Block Diagram

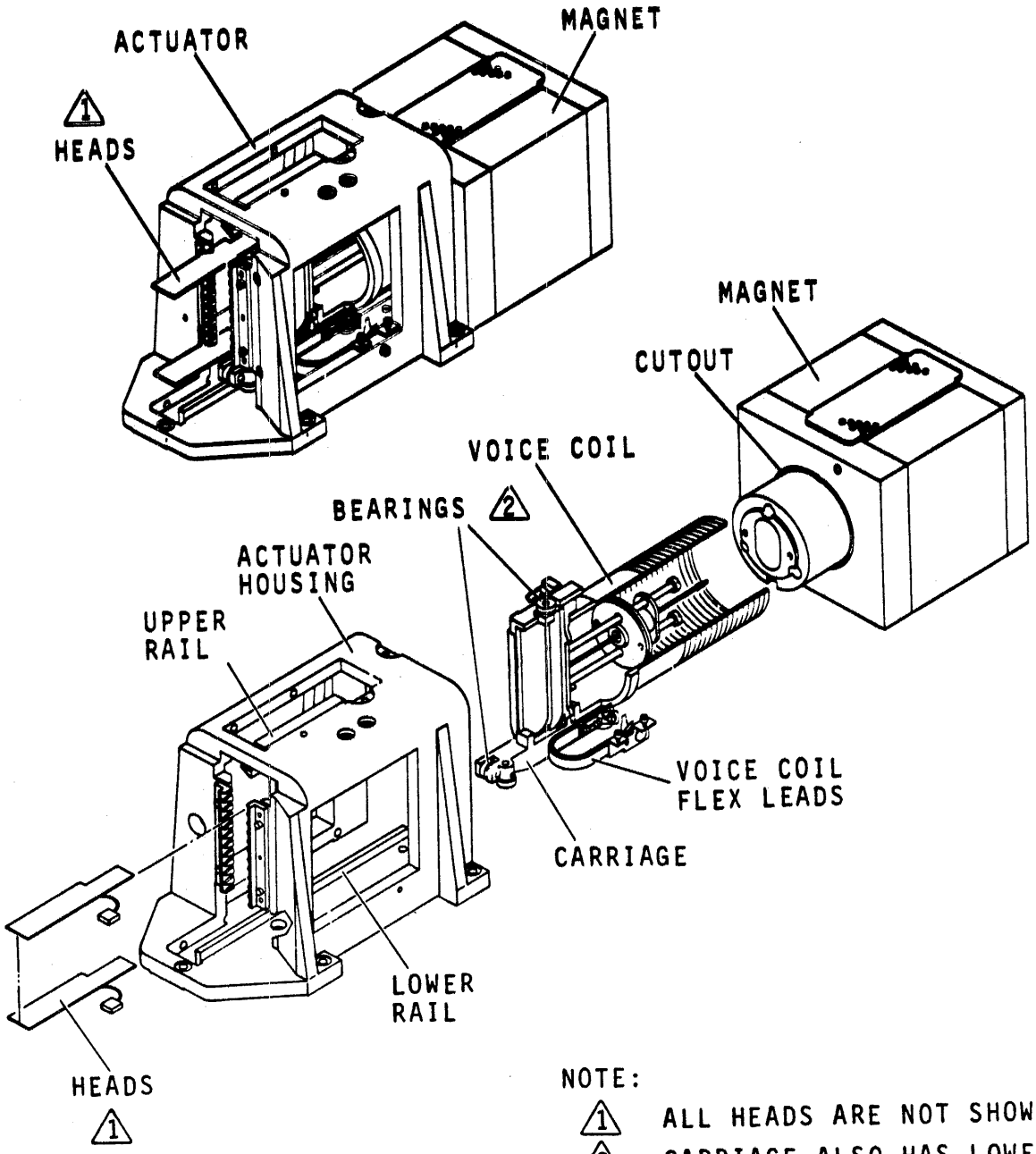

Figure 3-18. Actuator and Magnet Assembly

Actuator and Magnet Physical Description

The actuator and magnet are located on the rear half of the deck (refer to figure 3-18).

The actuator consists of the carriage and voice coil both of which are contained in the actuator housing. The carriage is mounted on bearings that allow it to move in a forward or reverse direction along rails attached to the actuator housing. The rear of the carriage forms a cylinder around which the voice coil is wrapped. The heads are mounted on the forward end of the carriage; therefore, the heads, carriage, and voice coil move together as a unit.

The magnet mounts directly behind the actuator and is a one piece assembly consisting of large permanent magnet. The magnet contains a circular cutout which allows the voice coil to move in and out of the magnet as the carriage moves.

Actuator and Magnet Functional Description

The movement of the carriage and voice coil (and therefore the heads) is controlled by positioning signals from the servo logic. The positioning signals are derived in the seek logic and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil via two flexible insulated metal strips called the voice coil flex leads.

The current from the power amplifier causes a magnetic field around the voice coil which reacts with the permanent magnetic field around the magnet. This reaction either draws the voice coil into the magnetic field or forces it away, depending upon the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

Velocity Transducer

The velocity transducer (refer to figure 3-19) mounts within the magnet and consists of a stationary coil and a movable magnetic core. The core is contained within the coil and connects to the carriage via an extension rod. Therefore, when the carriage moves, the motion is transferred via the extension rod to the core.

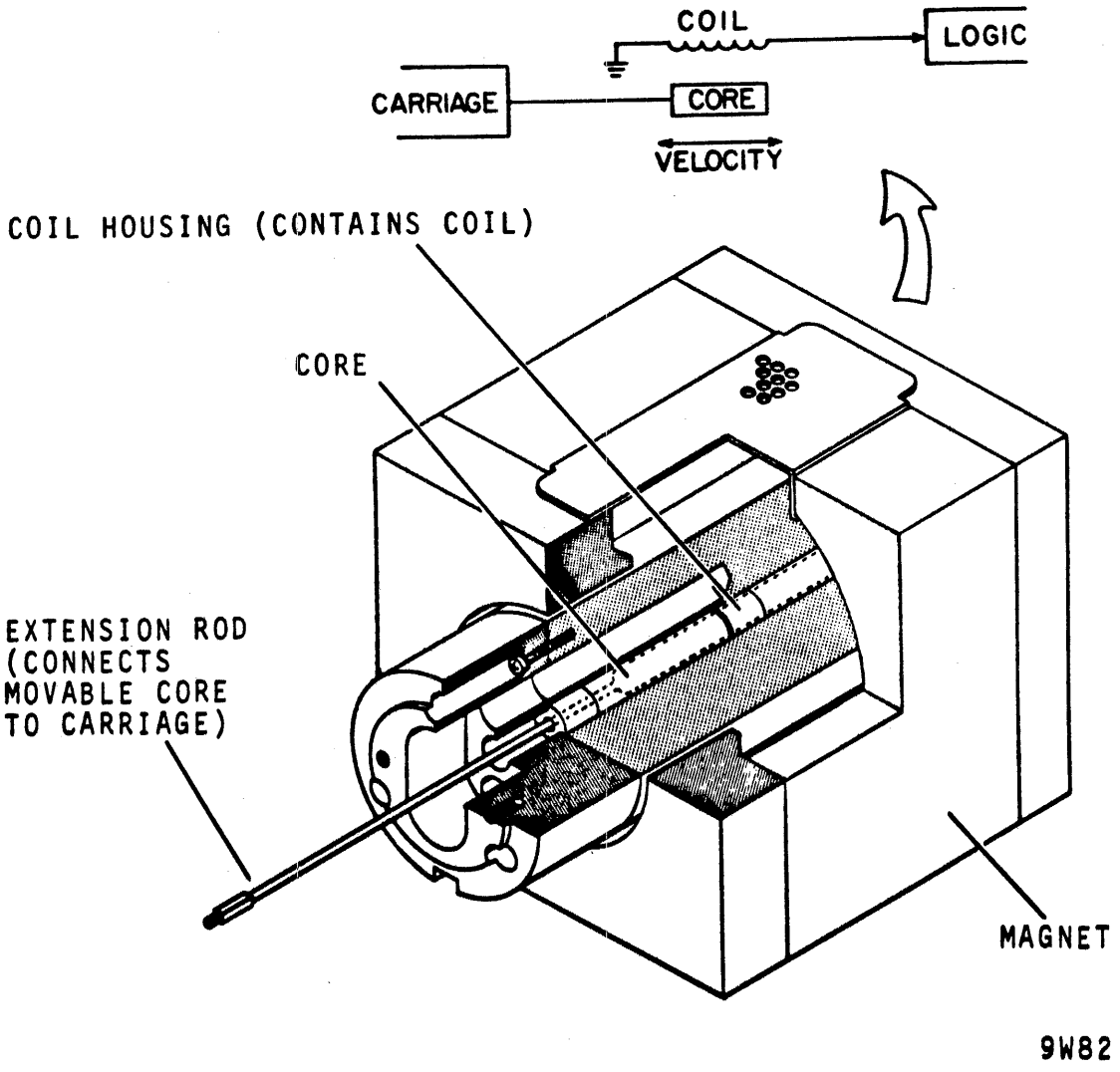

Figure 3-19. Velocity Transducer Assembly

When the carriage and core move, an EMF is induced in the coil. The amplitude of this EMF varies directly with the velocity of the carriage and the polarity of the EMF depends on the direction of carriage motion.

The output of the velocity transducer is sent to the servo logic which uses it to control the acceleration of the carriage during seek operations.

Heads Loaded Switch

The heads loaded switch (refer to figure 3-20) mounts in the actuator housing and indicates whether the heads are loaded or unloaded. This information is used by the seek logic and power on/off sequencing circuits.

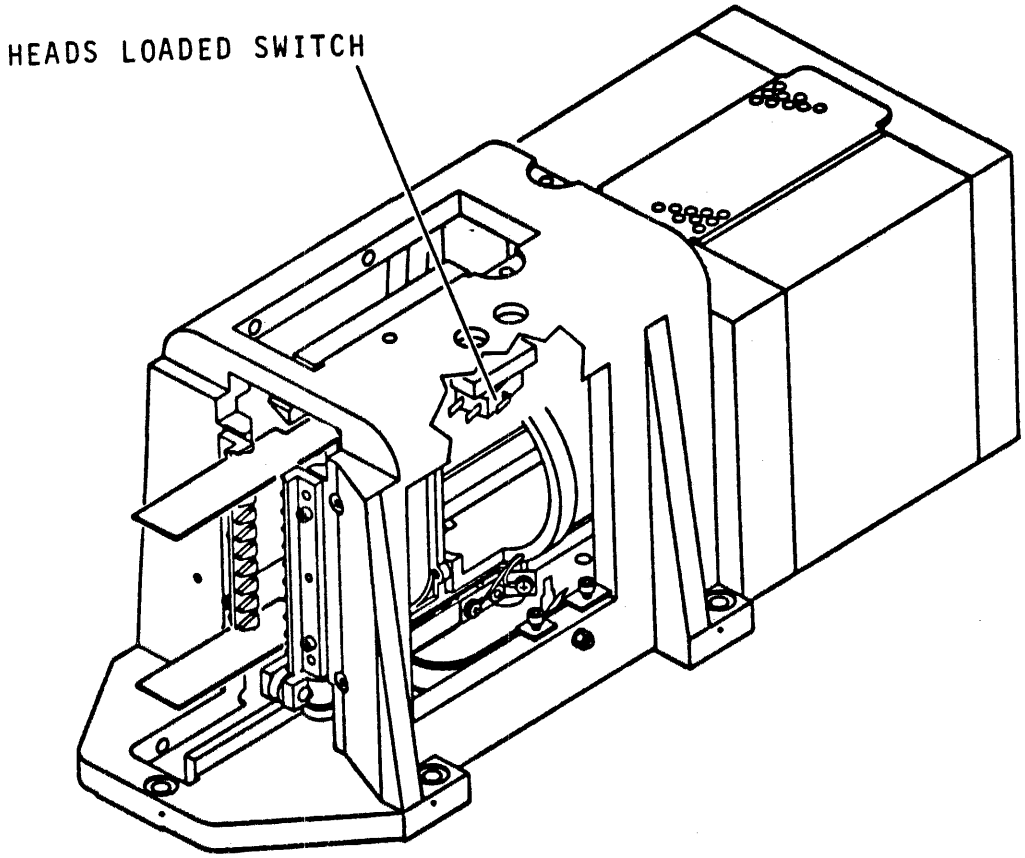

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Figure 3-20. Heads Loaded Switch Assembly

The switch is actuated by the carriage as the heads are loaded (moved out over the disk surfaces) or unloaded (moved clear of the disk surfaces and pack area). The switch indicates an unloaded status when the carriage is fully retracted and the heads are clear of the pack area.

During an unload sequence, the carriage retracts and transfers the switch, to indicate an unloaded condition, just as the heads leave the pack area.

HEADS

General

The heads are electromagnetic devices that record data on and read it from the disk pack. They are mounted in the end of a supporting arm and head and arm together are called a head-arm assembly. The head-arm assemblies attach to the carriage (refer to figure 3-21).

The drive has 20 heads, one for each disk surface. There are two types of heads (1) read/write and (2) servo. There are 19 read/write heads which are used to record data on and read it from the data surface. There is one servo head which is used to read information from the servo surface. This information is used by the drives servo circuits.

The following describes the physical characteristics of the head-arm assemblies and also how they function during head load and unload sequences. Further information concerning the heads

Head-Arm Assemblies Physical Description

Each head-arm assembly consists of a rigid arm, heads load spring, gimbal spring, and the head (refer to figure 3-22).
is found in the discussions on read/write and seek functions.

The rigid arm is mounted on the carriage and causes csrriage motion to be transmitted to the head. However, the arm does not provide the action necessary for the head to load, unload and follow the disk surface. This action is provided by the head load and gimbal springs.

The head load spring attaches to the rigid arm and is the mounting point for the gimbal spring. The head in turn attaches to the gimbal spring.

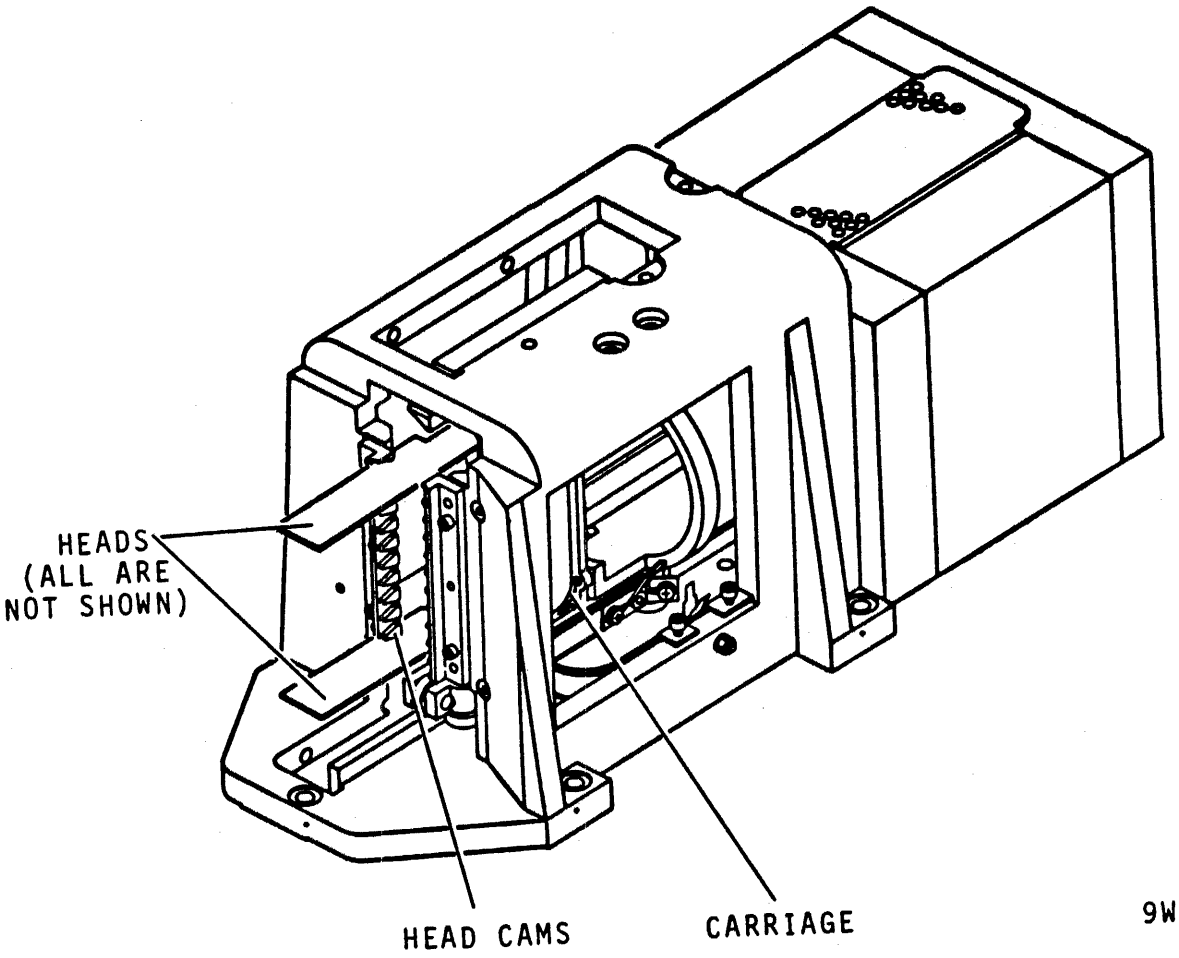

Figure 3-21. Heads

During head loading and unloading, the head load springs ride on the head cams and keep the heads from contacting one another. When the heads are loaded, the head load and gimbal springs work together and allow the heads to move independently of the rigid arms in the directions shown in figure 3-22. Such motion is necessary because when the heads are over the disk surfaces they do not contact the disk buyt actually fly on a cushion of air created by the spinning of the disk pack.

Information is sent to and from the heads via the head-arm cables. One end of each able connects to a head and the other end has a plug which connects to a card in the read/write chassis.

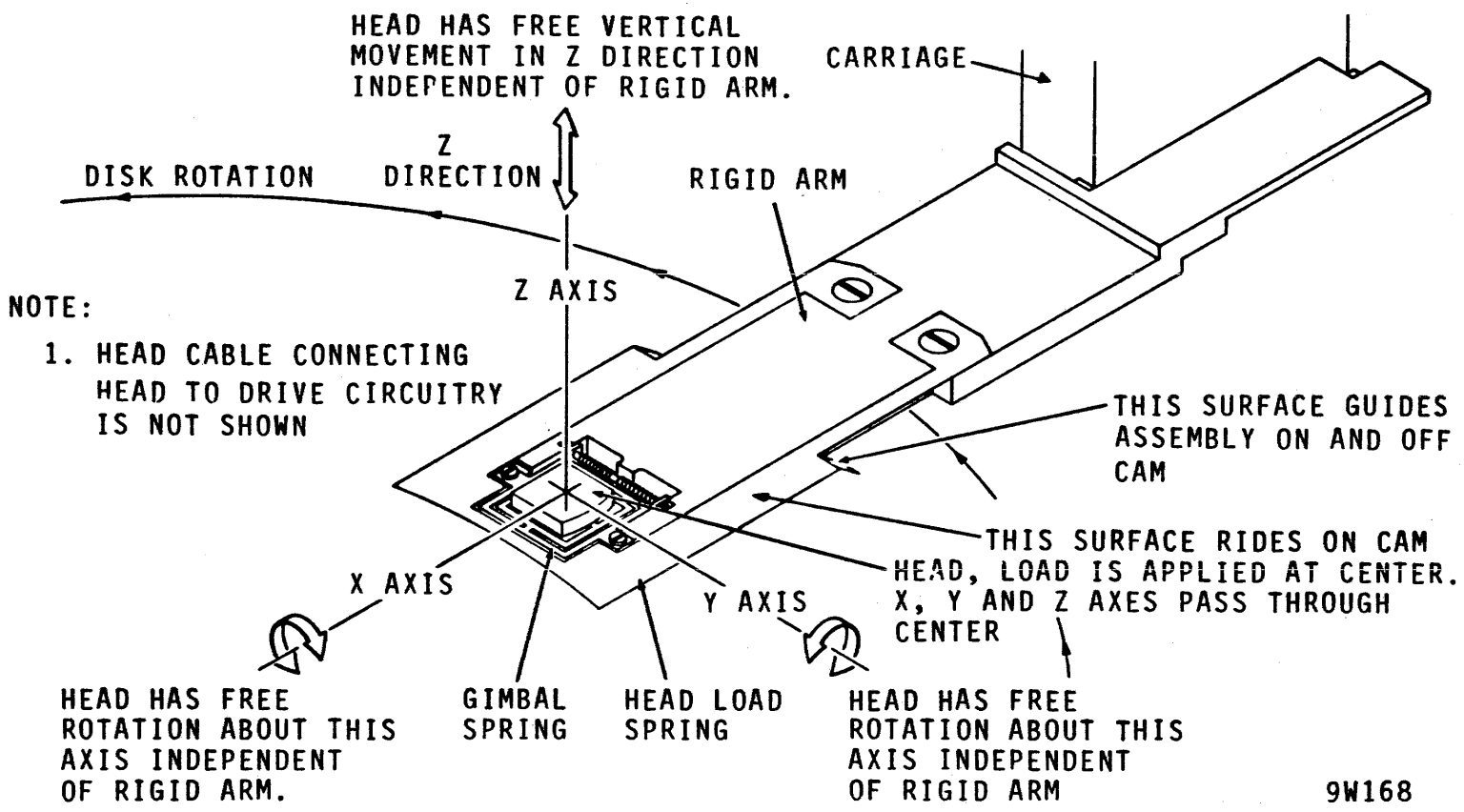

Figure 3-22. Head-Arm Assembly

Head Loading

The heads must be loaded before the heads can be positioned to a data track for the recording and reading of data. Loading the heads consists of moving them forward from their retracted (unloaded) positions until they are over the disk surfaces. All heads are loaded simultaneously.

The load sequence is initiated during the power up sequence when the disk pack has reached 3000 r/min. At this speed the spinning disk creates a sufficient cushion of air to allow the heads to fly.

When the pack is up to speed and the load logic is enabled, the heads move forward with the head load springs riding on the head cams. As the heads move out over the disk surfaces, the head load springs ride off the surfaces, of the head cams (refer to figure 3-23).

The load springs, while riding off the cams, unflex and force the heads toward the air cushions on the spinning disk surfaces. When the cushions of air are encountered, they resist any further approach by the heads. However, the head load springs continue to force the heads down until the opposing air and spring pressures are equal.

The air cushion pressure varies directly with disk speed and if the disk pack is rotating at the proper speed, the air and spring pressures should be equal when the heads are flying at the correct height above the disks.

If the disk pack drops below this speed, air cushion pressure decreases and the head load springs force the heads closer to the disks. Sufficient loss of speed causes the heads to stop flying and contact the disk surfaces.

Because insufficient disk speed causes head crash, loading occurs only after the disk pack is up to speed. For the same reason, the heads unload automatically if disk pack speed drops below a safe operating level (refer to discussion on emergency retract).

Head Unloading

The heads must be unloaded whenever the pack is stopped or if it is spinning too slowly to fly the heads. Unloading consists of retracting the heads until they are no longer over the disk surfaces.

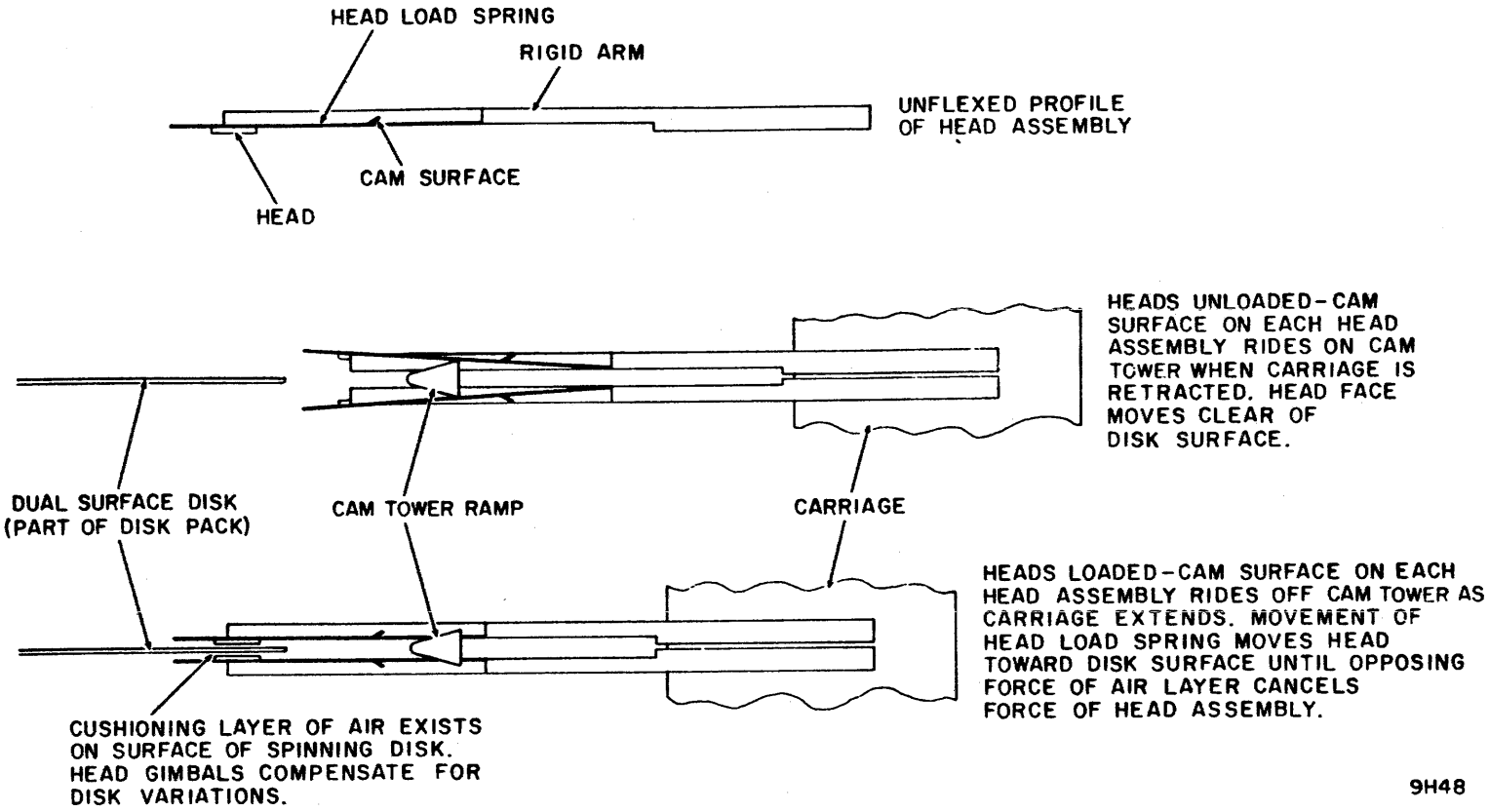

Figure 3-23. Head Loading

The unload sequence is initiated either during a normal power off sequence, or during an emergency retract function. In both cases current is applied to the voice coil that causes the carriage to move back towards the retracted stop.

As the carriage retracts, the head load springs encounter the head cam surfaces and the heads are pulled away from the disk surfaces. The carriage continues to move back until it is fully retracted.

AIR FLOW SYSTEM

The air flow system (refer to figure 3-24) provides ventilation and cooling air for the drive.

The heart of the air flow system is the blower assembly. This assembly consists of the blower motor, absolute filter, input port from primary filter and output ports to the logic chassis, power supply and pack area.

The blower motor provides the pressure needed to draw air into and push it through the system. The system intake port is located beneath the rear of the cabinet. This port is covered by the primary filter which keeps large particles from being drawn into the system. Air flows from the intake port through a duct in the floor of the cabinet to the blower motor.

The blower motor forces the air to the power supply, logic chassis, pack area and deck areas. The air to the logic chassis and power supplies, flows through hoses connected between these assemblies and the blower assembly. The air exhausted by the power supply and logic chassis circulates through the lower part of the drive cabinet and provides cooling air for the spindle motor.

The air to the pack area is filtered by the absolute filter which removes particles that might cause damage to the pack or heads. The air is forced into the pack area from all sides causing a positive pressure. This results in an upward dispersion of air, thus preventing the entrance of contaminated air through the pack access cover.

The air intake for the pack area is also forced into the deck area through vents in the rear of the shroud. This air cools the deck components and exits through vents on each side of the deck cover.

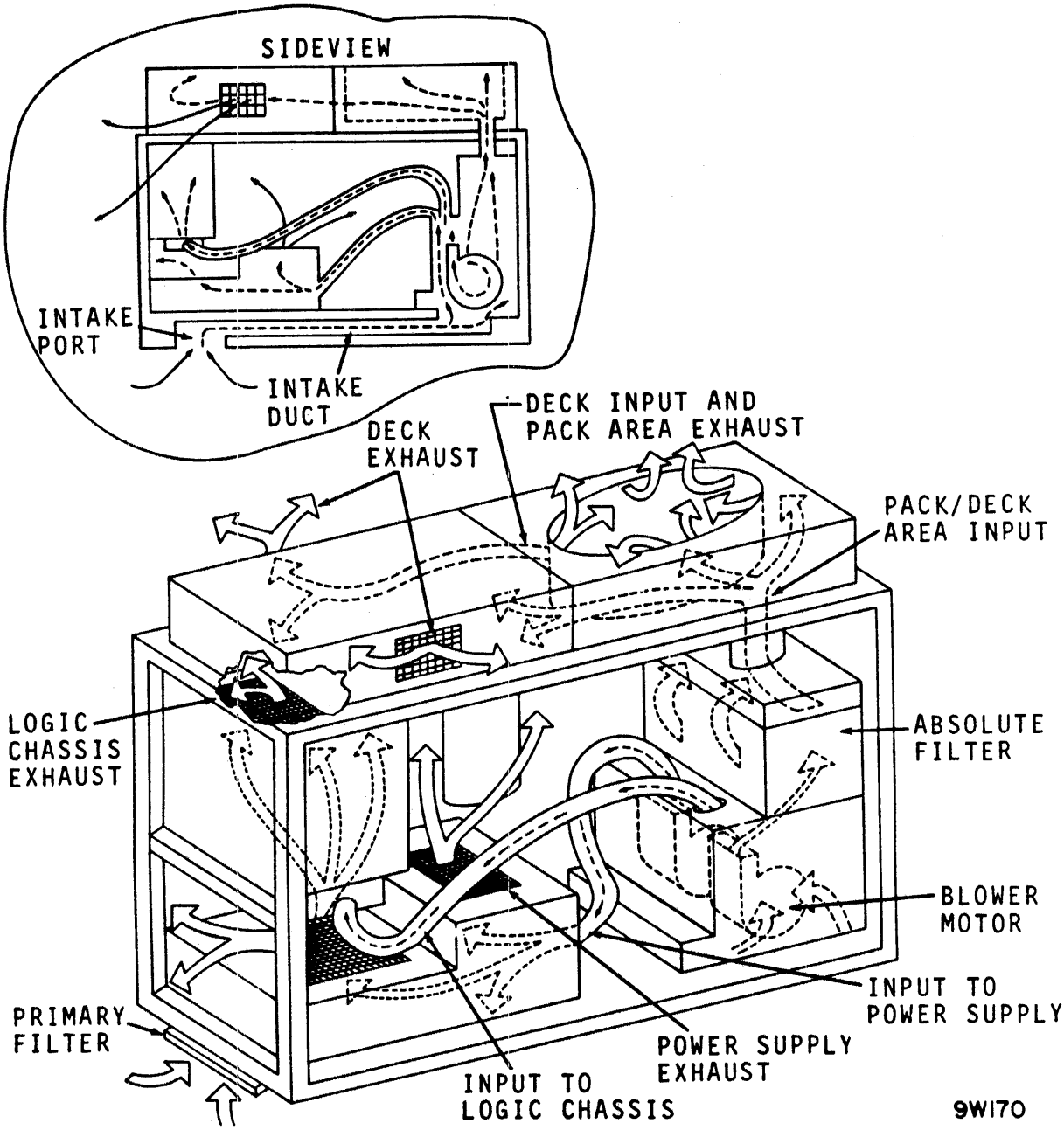

Figure 3-24. Air Flow System

INTERFACE FUNCTIONS

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals and read/write dasta transmitted and received by the drive.

The interface consists of the I/O cables and the logic required to carry and process the signals sent between drive and controller. The following describes both the I/O cables and I/O signal processing.

I/O CABLES

All the signal lines between the drive and controller are contained in two flat ribbon type I/O cables. They are referred to as the A and B cables.

The A cable contains lines connected in twisted pairs, which carry commands and control information to the drive and status information to the controller. This cable carries a maximum of 60 signals between drive and controller.

Figure 3-25 shows all lines in the A and B cables. The function of each of these lines is explained in tables 3-1 and 3-2.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations. The I/O signals are sent to the receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information, concerning the operation back to the controller via the transmitters. Figure 3-26 shows the basic logic involved in the routing of I/O signals.

All commands are sent to the drive via the tag and bus bit lines. These lines work in conjunction, the tag lines defining the basic operation to be performed and the bus bit lines further defining the basic operation. Table 3-1 explains the function of all tag and bus lines.

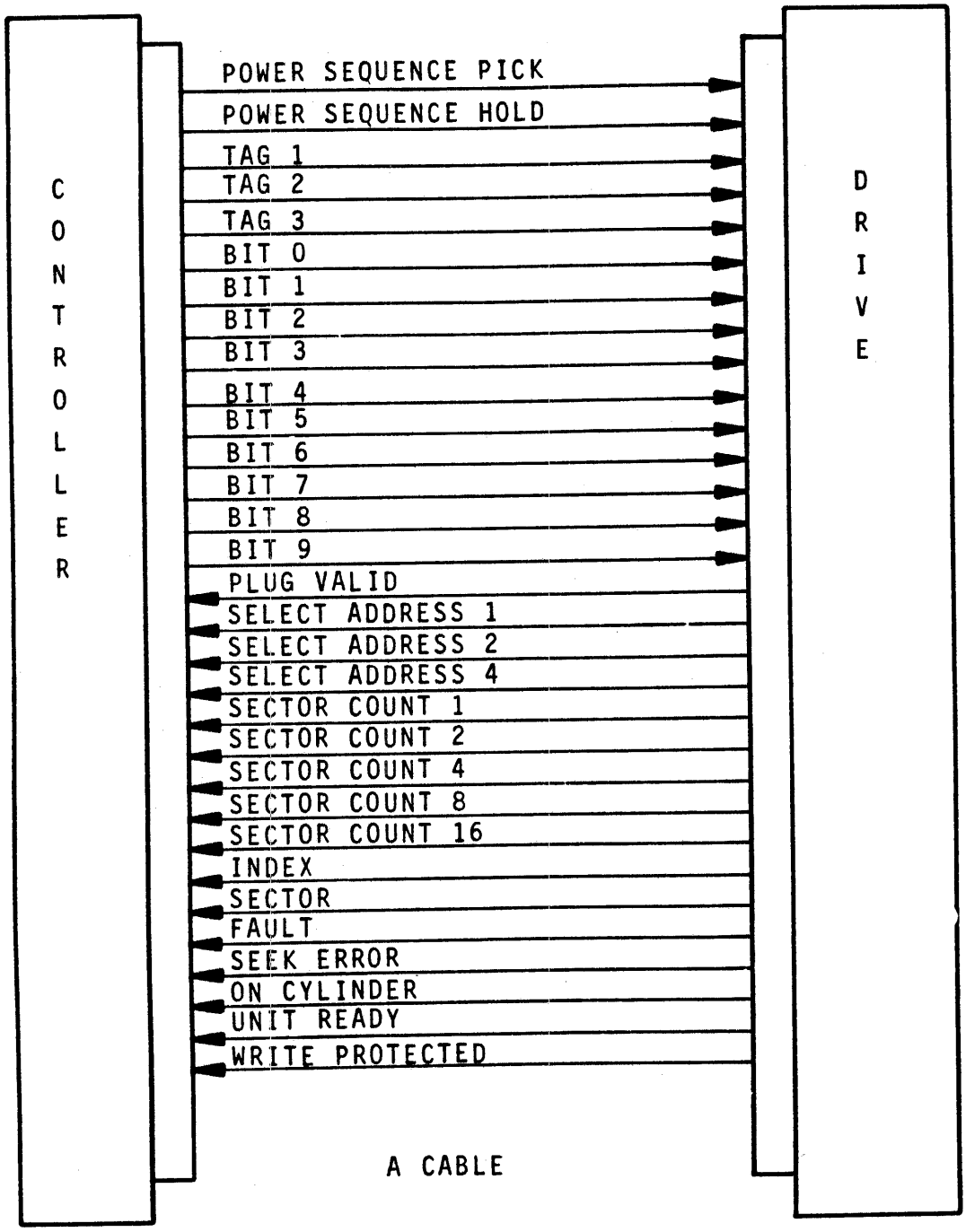

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Figure 3-25. I/O Cables (Sheet 1 of 2)

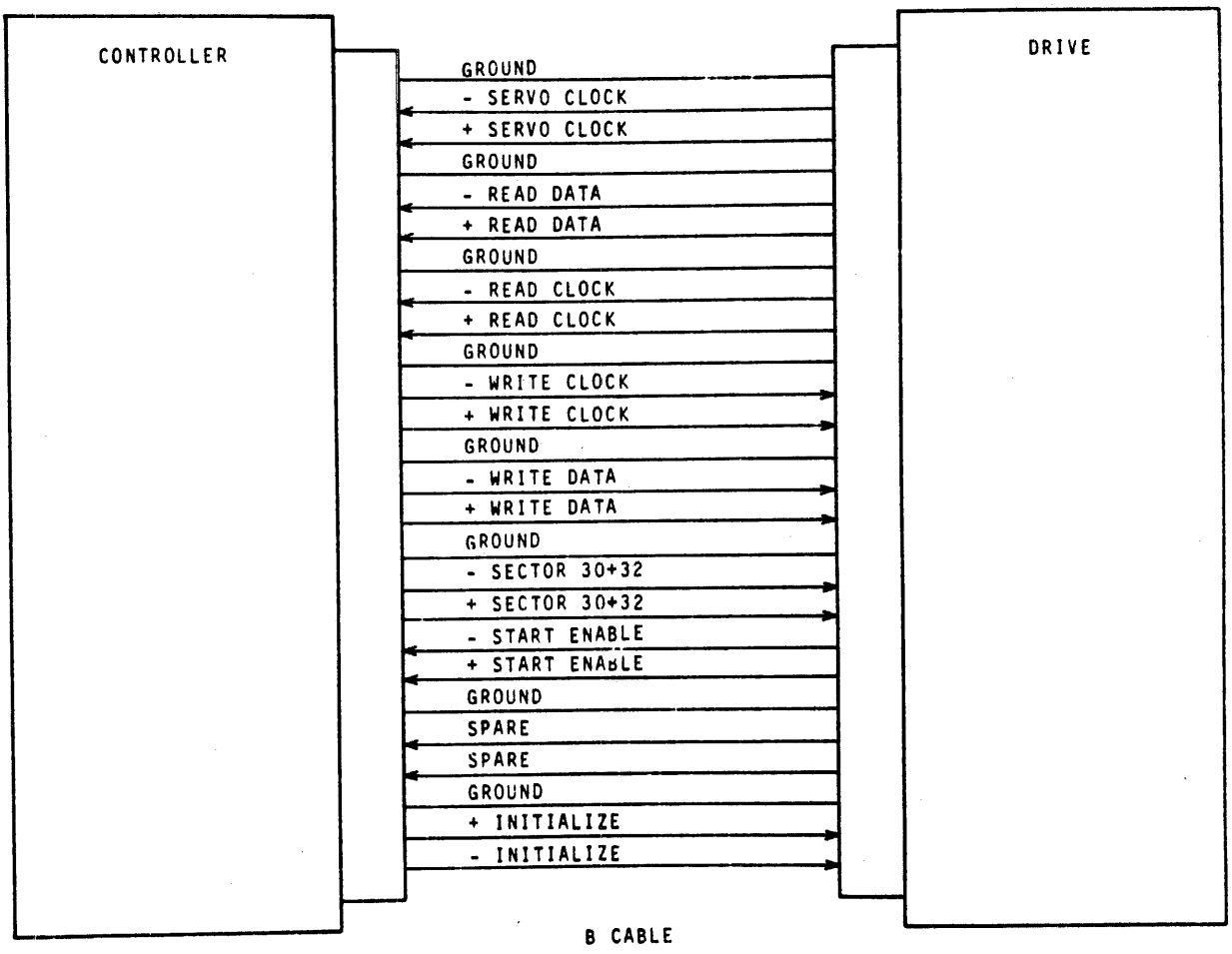


Figure 3-25. I/O Cables (Sheet 2)

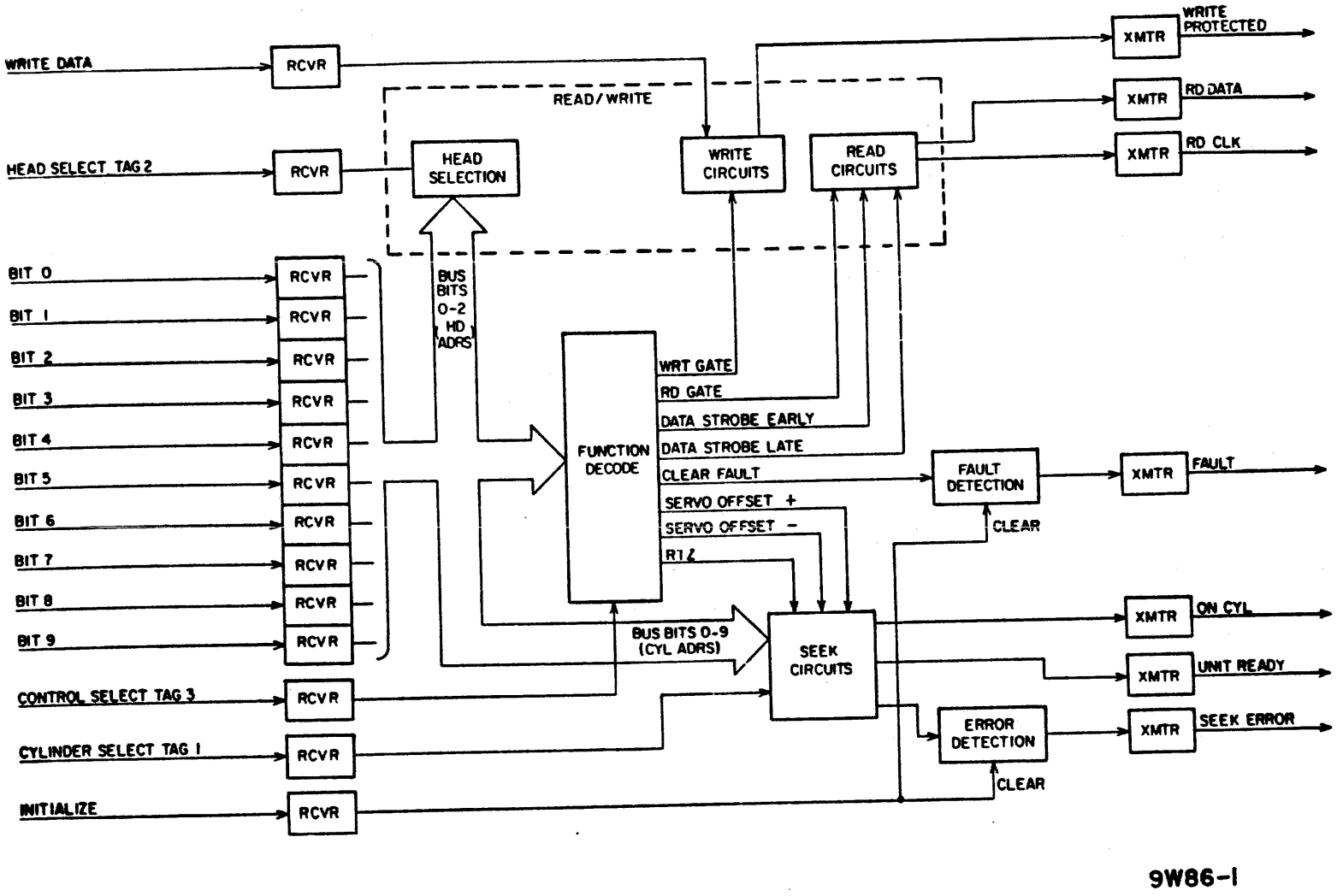


Figure 3-26. I/O Signal Processing (Sheet 1 of 2)

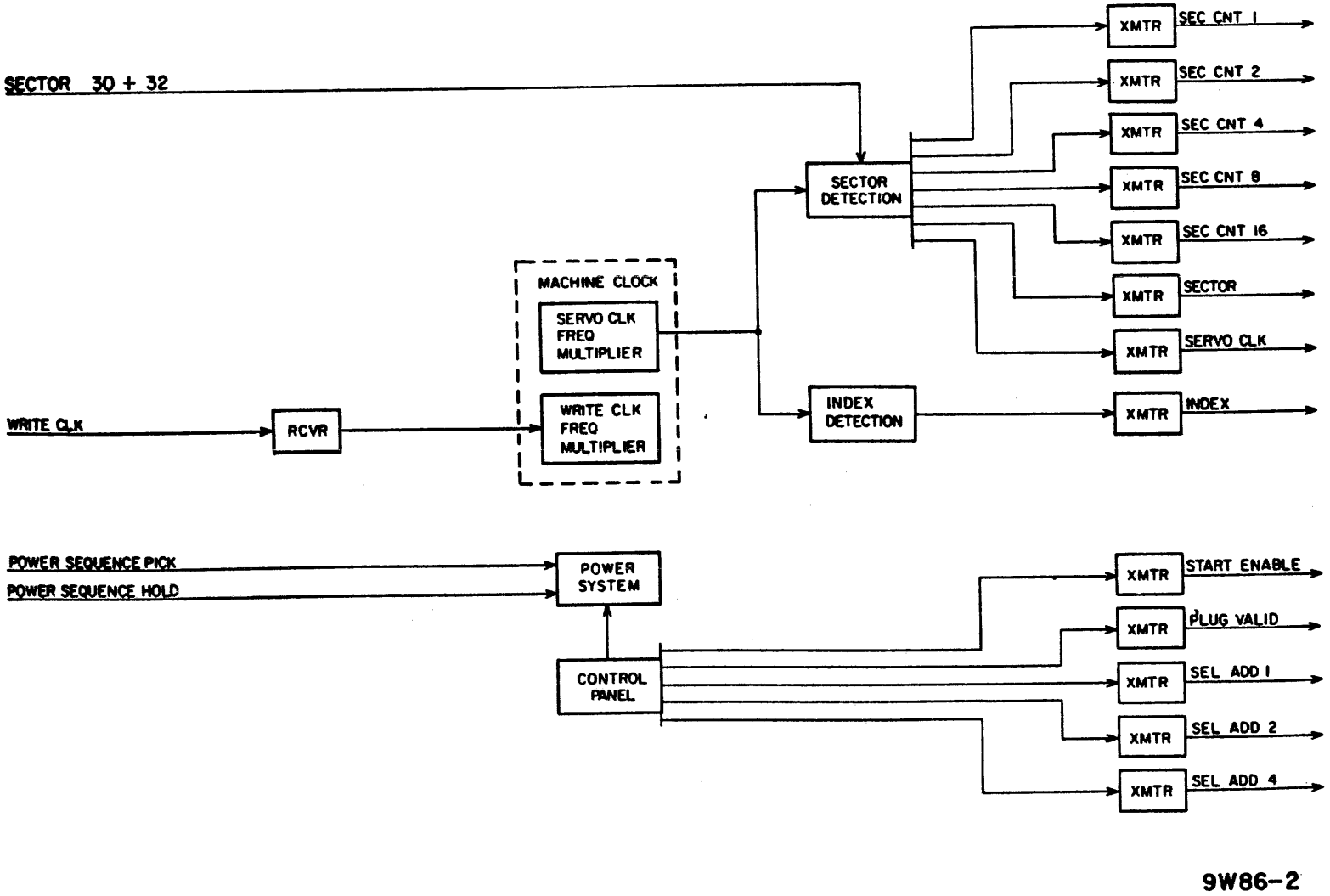


Figure 3-26. I/O Signal Processing (Sheet 2)

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS

Signal Line	Function
Power Sequence Pick (A Cable)	Used for power sequencing. A ground on this line powers up drive if LOCAL/REMOTE switch is in REMOTE and START switch is on (refer to discussion on Power Sequencing).
Power Sequence Hold (A Cable)	Used for power sequencing. This line must be grounded at controller for drive to complete and hold remote power up sequence (refer to discussion on Power Sequencing).
Cylinder Select Tag 1 (A Cable)	Used in conjunction with Bus Bit lines to initiate seek function. This tag strobes the cylinder address, contained in Bus Bit lines, into drive logic. Drive must be on cylinder before this tag is sent. Bus Bits are interpreted as follows: Bus Bit — Function 0 — Cyl Adrs Bit 0 1 — Cyl Adrs Bit 1 2 — Cyl Adrs Bit 2 3 — Cyl Adrs Bit 3 4 — Cyl Adrs Bit 4 5 — Cyl Adrs Bit 5 6 — Cyl Adrs Bit 6 7 — Cyl Adrs Bit 7 8 — Cyl Adrs Bit 8 9 — Cyl Adrs Bit 9

Table Continued on Next Page

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS (Contd)

Signal Line	Function
Head Select Tag 2 (A Cable)	Used in conjunction with Bus Bit lines to initiate head select function. This tag strobes the head address, contained on Bus Bit lines, into drive logic. Bus Bits are interpreted as follows: Bus Bit — Function 0 — Head Adrs Bit 0 1 — Head Adrs Bit 1 2 — Head Adrs Bit 2 3 — Head Adrs Bit 3 4 — Head Adrs Bit 4 5-9 — Not Used
Control Select Tag 3	Initiates various operations to be performed by the drive. Used in conjunction with Bus Bit lines, which operation is initiated depends on content of these lines which are defined as follows: Bus Bit — Function 0 — Write Gate - Enables write drivers. 1 — Read Gate - Enables the digital read data lines. Leading edge triggers read chain to sync on all-zeros pattern.

Table Continued on Next Page

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS (Contd)

Signal Line	Function
	2 Servo Offset Positive - Offsets the actuator from the nominal on cylinder position toward the spindle.
	3 Servo Offset Negative - Offsets the actuator from the nominal on cylinder position away from the spindle.
	4 Fault Clear - A 100 ns (minimum) pulse sent to drive. Clears the Fault Latch if fault condition no longer exists.
	5 Not Used
	6 RTZ Seek - A pulse (250 ns to 1.0 ms wide) sent to drive to cause actuator to seek to track zero, clear head address register, and clear seek error latch.
	7 Data Strobe Early - Enables the PLO data separator to strobe the data at a time earlier than optimum.
	8 Data Strobe Late - Enables the PLO data separator to strobe the data at a time later than optimum.
	9 Not Used
Bus Bits 0 - 9 (A Cable)	Used in conjunction with Tags 1, 2 and 3 to define commands to the drive.
Write Data (B Cable)	Carries NRZ data to be recorded on disk pack.

Table Continued on Next Page

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS (Contd)

Signal Line	Function
Write Clock (B Cable)	Synchronized to NRZ Write Data, it is a return of the Servo Clock. This signal is transmitted continuously.
Sector 30 + 32 (B Cable)	Used to determine the number of sectors per revolution. When line is high, there are 32 sectors per revolution. When line is low, there are 30 sectors per revolution (refer to track orientation discussion).
Initialize (B Cable)	Clears the Fault, Voltage Fault, and Seek Error latches provided the errors no longer exist.

UNIT SELECTION

Unlike drives that have common interface lines connecting them to the controller, each BK7 drive has unique I/O lines connecting it to the controller. Therefore, the controller does not select a particular drive before placing a command for it on the I/O lines. However, the controller must receive certain signals from a drive before issuing a command to it. The sequence of these signals appears in the flowchart in figure 3-27. When the drive has completed its power on sequence and has sent these signals to the controller, it will respond to every command appearing on its I/O lines.

SEEK FUNCTIONS

GENERAL

The drive must move the heads to the desired position over the disk pack before any read or write operation can be performed. This is done during seek functions and is performed by the drive's servo circuits.

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTION

Signal Line	Function
Plug Valid (A Cable)	Used to indicate that a logic plug is installed in the control panel.
Select Address 1,2,4 (A Cable)	Three lines which carry the binary coded logical address of the drive. The logical address is controlled by the logical address plug installed in the control panel. There are eight valid addresses (plugs 0 through 7).
Sector Count 1,2,4, 8, and 16 (A Cable)	Five lines which carry the binary coded sector address. The output on the lines represents the contents of the Sector Address register. The sector count changes on the leading edge of either Index Detection).
Index (A Cable)	Occurs once per revolution of disk pack and its leading edge is considered leading edge of sector zero (refer to discussion on Index Detection).
Sector (A Cable)	Derived from servo surface of disk pack, this signal can occur either 30 or 32 times per revolution of disk pack. The number of sector pulses occuring depends on the condition of the Sector 30 or 32 line from the controller.
Fault (A Cable)	Indicates that one or more of the following faults exist; write fault, multiple head select fault, write and read fault, voltage fault, read or write and not on cylinder.

Table Continued on Next Page

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTION (Contd)

Signal Line	Function
Seek Error (A Cable)	Indicates that the unit was unable to complete a move within 500 ms, or that carriage has moved to a position outside recording field. A seek error is also generated if an address greater than cylinder 822 has been selected.
On Cylinder (A Cable)	Indicates drive has positioned the heads over a track (refer to discussion on seek functions).
Unit Ready (A Cable)	Indicates that drive is selected, disks are up to speed, heads are loaded, and no fault conditions exists.
Write Protected (A Cable)	Indicates that drives write circuits are disabled. Write Protected is active under any of the following conditions: head alignment is being performed, a Fault condition exists, WRITE PROTECT switch on control panel is activated.
Servo Clock (B Cable)	9.667 MHz clock signals derived from servo track dibits (refer to discussion on Machine Clock).
Read Data (B Cable)	Carries NRZ data recovered from disk pack (refer to discussions on Read/ Write functions).
Read Clock (B Cable)	Clock signals derived from NRZ Read Data (refer to discussions on Read /Write functions).
Start Enable (B Cable)	Reflects the condition of the START switch. When the switch is in the start condition the line is active.

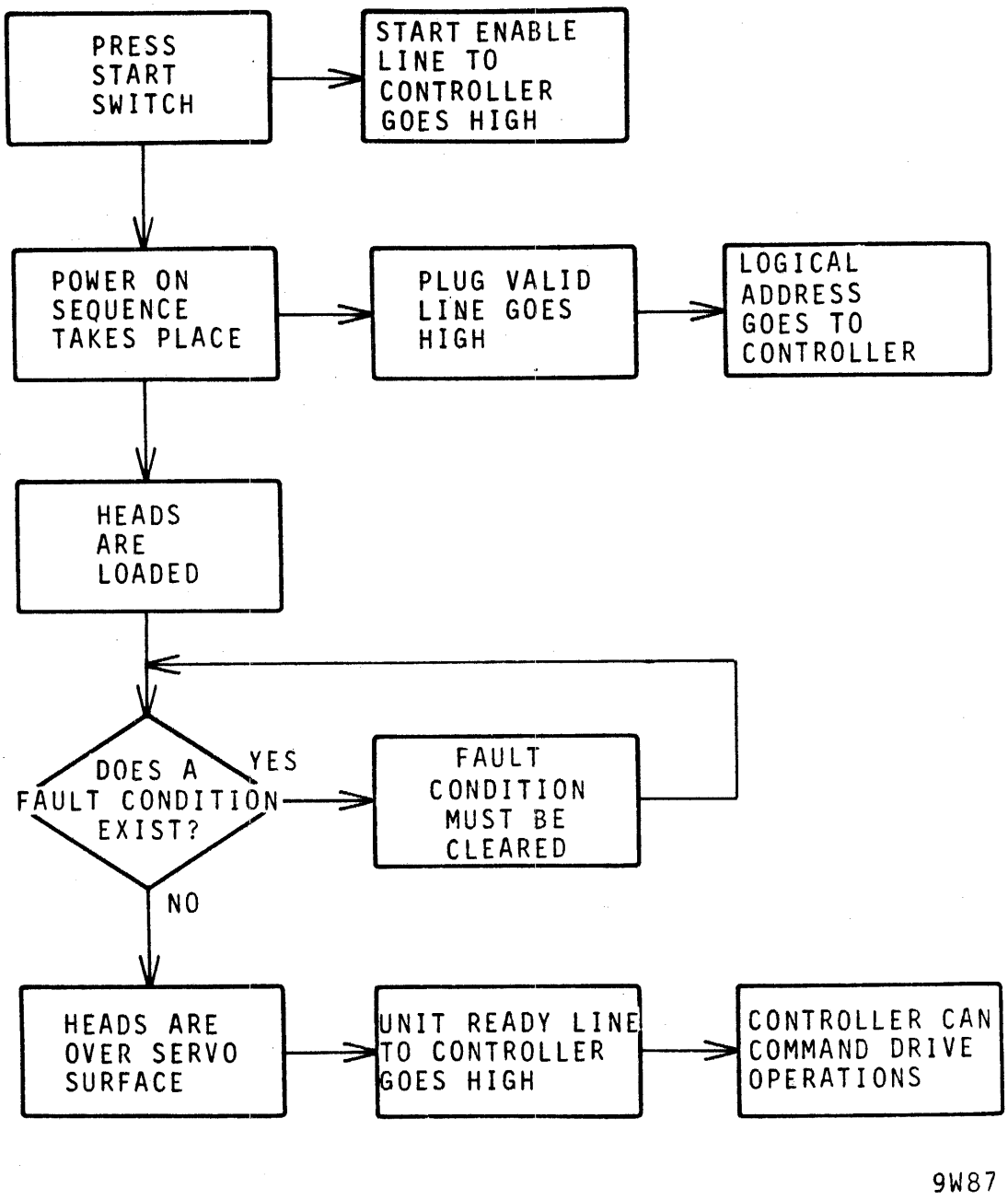


Figure 3-27. Unit Selection Flowchart

The servo circuits form a closed-loop servo system that controls movement by comparing the present position of the heads to the desired future position and generating a position control signal proportional to the difference between them.

The major elements in the servo loop are shown on figure 3-28. The drive servo loop, the circuits it contains, and how it works during seek functions, are described in the following discussions. These discussions are organized as follows:

- Overall Loop Description - Provides overall explanation of servo loop and how it functions during various seeks.
- Servo Disk Information - Describes the information that is permanently recorded on the servo surface of the disk pack and used by the servo loop to control positioning.
- Position Feedback Generation - Explains how the servo disk information is converted to feedback signals that control positioning of the heads.
- Velocity Feedback Generation - Explains how the speed of the carriage is monitored and how this information generates signals to control the speed of the carriage.
- Position Signal Amplification - Explains how the position signals from the position control circuits generate current for the voice coil.
- Direct Seek Position Control - Explains how the positioning signals are generated and how the overall loop functions during direct seek sequences.
- Load Seek Position Control - Explains how the positioning signals are generated and how the servo loop functions during load seeks. These occur during the power up sequence when the heads are loaded.
- Return-to-Zero Seek Position Control - Explains how the positioning signals are generated and how the servo loop functions when the controller commands a return-to-zero (RTZ) seek.
- Unload Seek Position Control - Explains how the positioning signals are generated and how the servo loop functions during power off sequences when the heads unload.
- Seek End and Seek Error Detection - Describes the indications sent to the controller at the end of a seek and also describes the various seek errors detected by the drive.

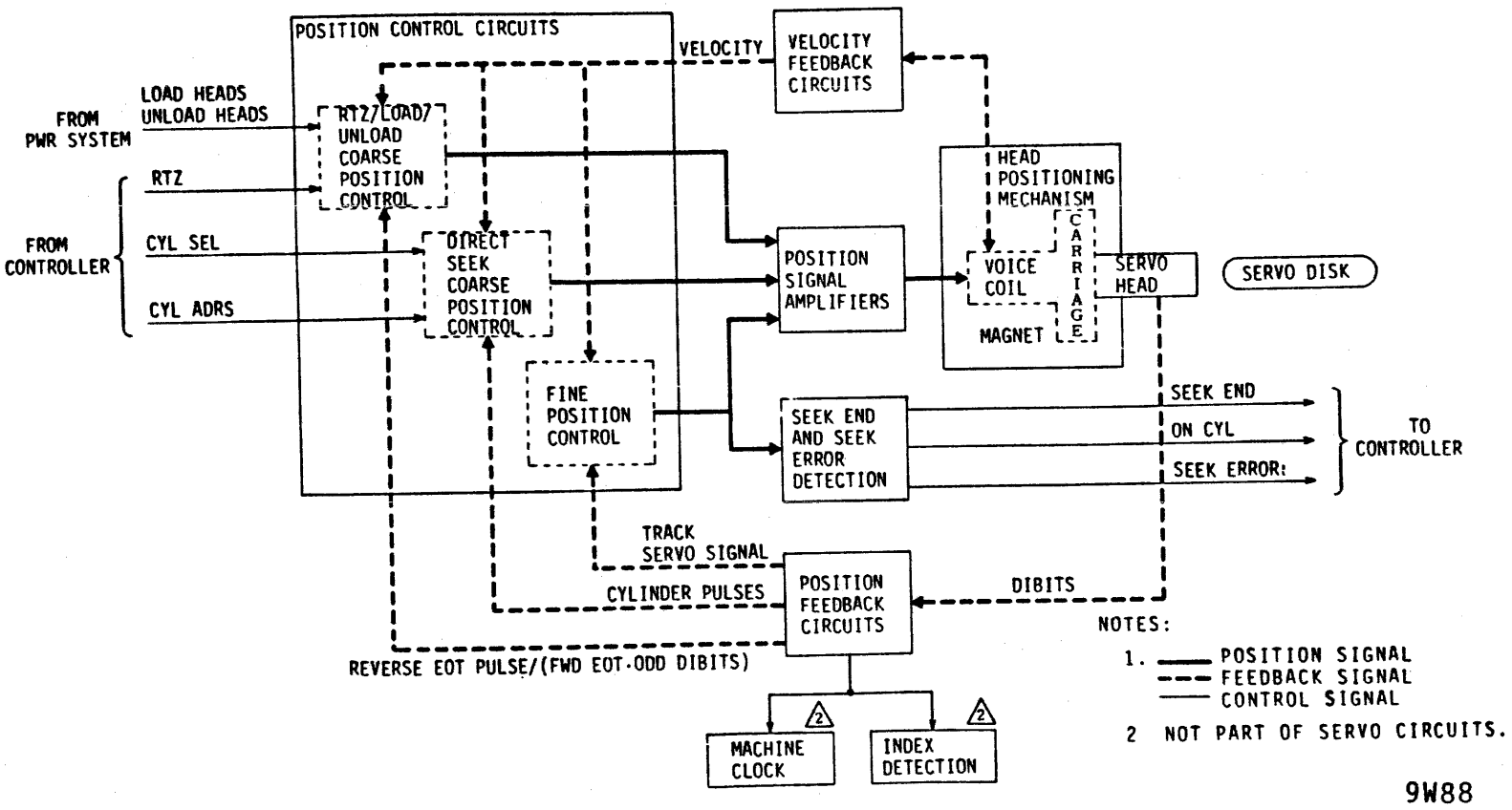


Figure 3-28. Servo System Functional Block Diagram

OVERALL LOOP DESCRIPTION

The servo loop (refer to figure 3-28) consists of the position control circuits, position signal amplifiers, head positioning mechanism, and feedback circuits (both velocity and position).

The inputs to the loop are applied to the position control circuits. These inputs come either from the controller (in the case of a direct or return-to-zero seek) or from the power system (in the case of a load or unload sequence). This is explained further in the discussions on position control.

The position control circuits are divided into three parts (1) RTZ (return-to-zero)/load/unload coarse position control (2) direct seek coarse position control and (3) fine position control. Which of these controls positioning depends on the type of seek being performed and how close the heads are to the desired position. The following explains the action of the position control circuits and the rest of the servo loop during a typical seek operation.

At the start of a seek, the initial positioning information is input to either the RTZ/load or direct seek coarse position control circuits (depending on the seek being performed). These circuits then generate a control signal proportional to the distance to the destination. The signal polarity depends on the direction of the seek.

The position control signal is processed by the position signal amplifier, which uses it to generate current for the voice coil. The voice coil is attached to the carriage, which is the device that supports and moves the heads. The voice coil is within a magnet and whenever a current passes through the coil windings, the interaction between the induced EMF and the magnetic flux field causes the voice coil and carriage to move. The acceleration of the motion is proportional to the polarity and magnitude of the voice coil current (the head positioning mechanism is discussed in detail in the discussions on Electromechanical Functions).

As the heads move, feedback signals are generated that indicate how fast the heads are moving (velocity feedback) and how far the heads have moved toward the desired destination (position feedback).

The velocity information is derived from the velocity transducer, which generates signals proportional to carriage speed. The position feedback signals are generated from information read from the servo disk by the servo head.

Both velocity and position feedback signals are used by the coarse position feedback circuits to vary the position control signal as the destination is approached. They are also used to determine when the servo system should switch from coarse to fine control.

When this switch is made, the coarse position control circuits are disabled and the fine position circuits are enabled. Fine control is necessary to ensure that the heads are accurately positioned over the destination and also to keep it positioned once the seek is complete. The fine position control circuits also use signals from the feedback circuits to control positioning.

The seek-end and seek-error detection circuits sense when the seek is complete and at this time indicate if the seek was successful.

The preceding described basic loop operation. More detailed descriptions of the elements in the loop and loop operation are contained in the following discussions.

SERVO DISK INFORMATION

GENERAL

The servo disk surface (refer to figure 3-29) contains servo ositioning information that is recorded on the disk at the time of manufacture.

This information is read by the servo head and processed by the position feedback circuits. These circuits generate position feedback signals that are used by the positioning circuits to control the positioning of the heads. The servo disk information also generates clock signals used by the Index and Machine clock circuits.

This discussion describes the servo disk information and is divided into the following areas:

- Dibits
- Dibit tracks
- Outer and Inner Guard Bands
- Servo Zones
- Cylinder Concepts

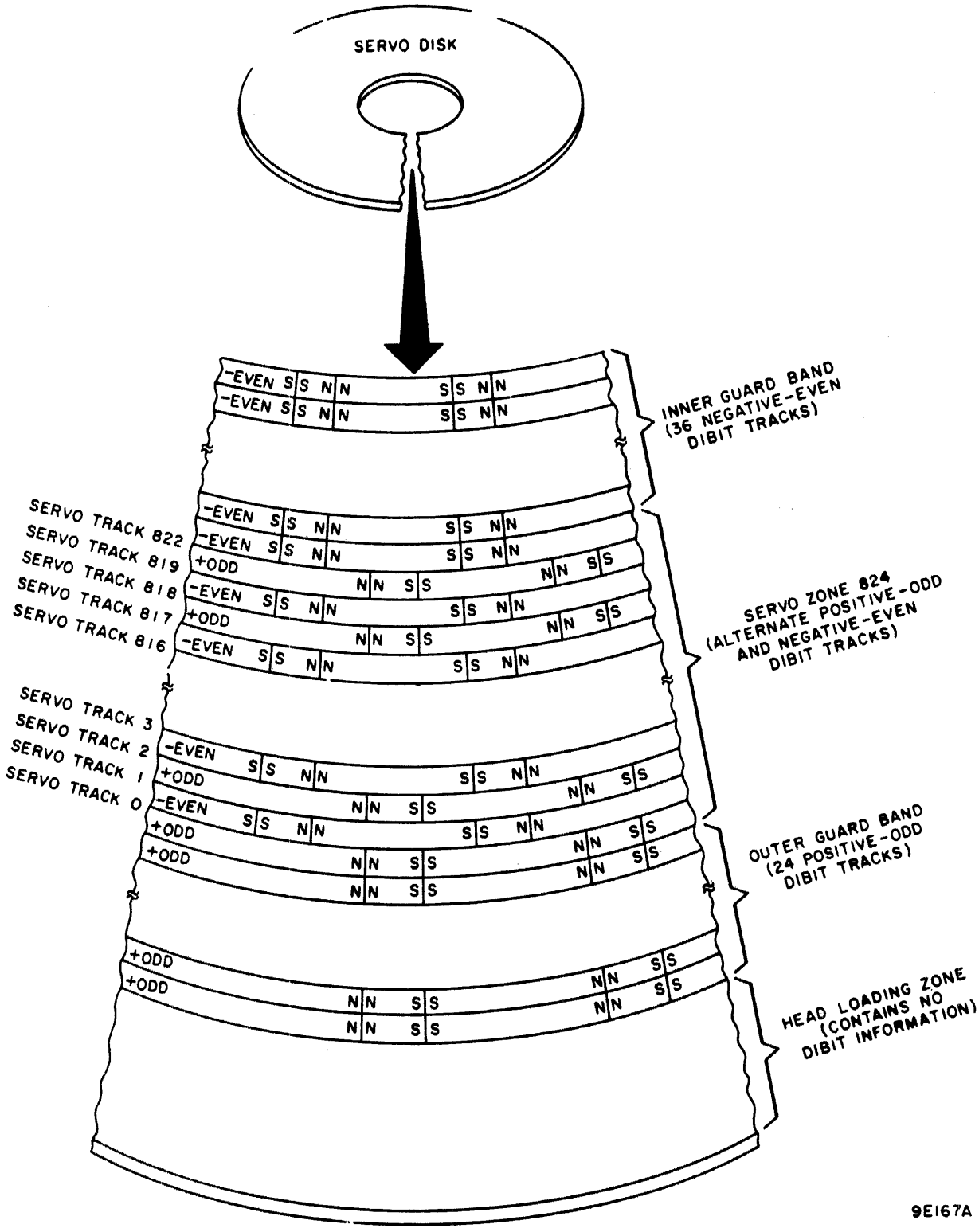


Figure 3-29. Servo Disk Format

Dibits

The servo positioning information is recorded on the disk as specific patterns of flux reversals referred to as dibits. There are two types of dibits: positive and negative.

The positive and negative dibits are classified according to the type of waveform produced when they are read by the servo head (the waveform actually appears at the output of the track servo preamp). The positive dibits produce a waveform with the leading pulse positive and the trailing pulse negative. The negative dibits produce a waveform with the leading pulse negative and the trailing pulse positive. The dibit patterns and their associated waveforms are shown on figure 3-30.

Dibit Tracks

The dibits are recorded in track patterns around the disk. The servo surface has 833 dibit tracks, each recorded exclusively with either positive or negative dibits. These tracks are recorded adjacent to one another with no void area between them. Those tracks containing only positive dibits are known as positive-odd dibit tracks and those tracks containing only negative dibits are known as negative-even dibit tracks.

Outer and Inner Guard Bands

The outer 24 tracks are positive-odd dibit tracks and contain only positive dibits. This area is known as either the outer guard band or the reverse end of travel (reverse EOT).

The inner 36 tracks are negative-even dibit tracks and are known as either the inner guard band or the forward end of travel (forward EOT).

Both the outer and inner guard bands are shown on figure 3-29.

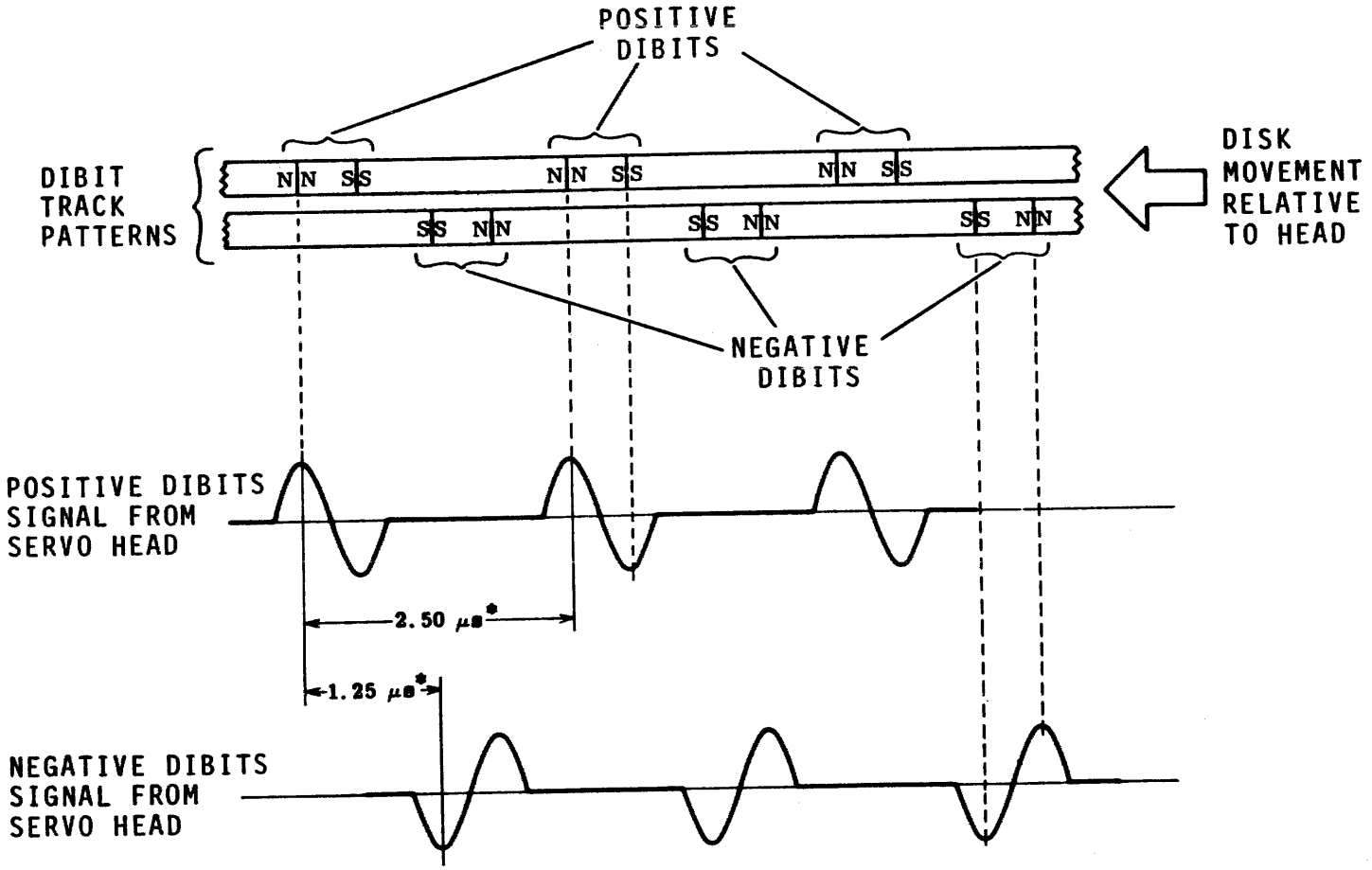


Figure 3-30. Positive and Negative Dibit Pattern

Servo Zones

In between the inner and outer guard bands is an area called the servo zone. The servo zone consists of alternately spaced positive-odd and negative-even dibit tracks. Because the dibit tracks are adjacent to one another, junctions are formed between the positive and negative tracks. These junctions are referred to as servo tracks. The servo zone contains 823 servo tracks, numbered from 000 to 822.

When the servo head is centered over a servo track, it will alternately detect both positive and negative dibits. The combination of these signals results in each servo track being divided into exactly 13 440 intervals (where an interval is the time between the leading peaks of successive dibits).

In addition to this, each dibit track in the servo zone is encoded with a pattern of missing dibits and this results in each servo track also containing a pattern. This pattern, referred to as Index, is the same on each servo track and is recorded at a specific circumferential location on the tracks.

Further information about Index and its application is given in the discussions on Track Orientation.

Cylinder Concept

The data recording zones on the data surfaces are aligned vertically with the servo track zone on the servo surface. For this reason, all head movement and positioning is referenced to the position of the servo head over the servo surface.

Therefore, when the servo head is positioned over a specific servo track on the servo surface, all other heads are positioned over the corresponding data tracks on their respective data surfaces. For example, if the servo head is over track 10, all other heads are also over track 10. The vertical alignment of these tracks create an imaginary cylinder as shown on figure 3-31.

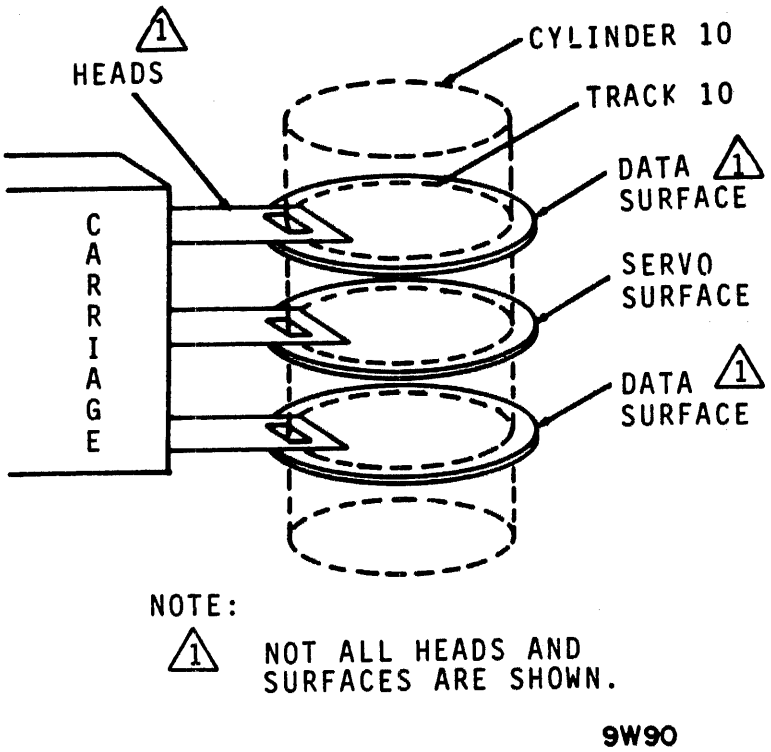


Figure 3-31. Cylinder Concept

POSITION FEEDBACK GENERATION

General

All position feedback information is generated by the position feedback circuits. These circuits use the dibit data read from the servo disk to generate the feedback signals required by the position control circuits.

The feedback signals generated and their basic functions are as follows:

- Track Servo signal - Used by the fine position control circuits to control positioner movement during the last half track of a seek.

- Cylinder Pulses - Pulses that occur each time the servo head crosses a servo track. These pulses are used by the coarse position control to determine the distance to the desired cylinder.

- Reverse EOT Pulse - Provides feedback to the RTZ coarse position control circuits during a return to zero seek (RTZS).

- Forward EOT Enable and Odd Dibits - Provides feed back during RTZ, Load, and Unload seeks that cause positioning control to be switched from the RTZ, Load, and Unload coarse position control circuits to the fine position control circuits.

In addition to providing these signals, the position control feedback circuits also produce the Odd/Even dibit signals used by the Machine Clock and Index Detection circuits.

A basic block diagram of the position feedback circuits is shown on figure 3-32 and each of the following elements are explained in the following discussions:

- Track Servo Preamp
- Dibit Sensing
- Automatic Gain Control (AGC)
- Track Servo Signal Amplifier
- Odd/Even Dibit Clock Generation
- Cylinder Crossing Detection
- End of Travel Detection

Track Servo Preamp

This signal from the servo head must be processed by the track servo preamplifier before the servo track information can be used by the rest of the position feedback circuits.

The signal received from the servo head depends on the type of servo dibit track it is reading. When the head is over the outer or inner guard bands, it reads from tracks that have either all positive or all negative dibits. In this case, the preamp produces either all positive or all negative dibit waveforms (refer to figure 3-30).

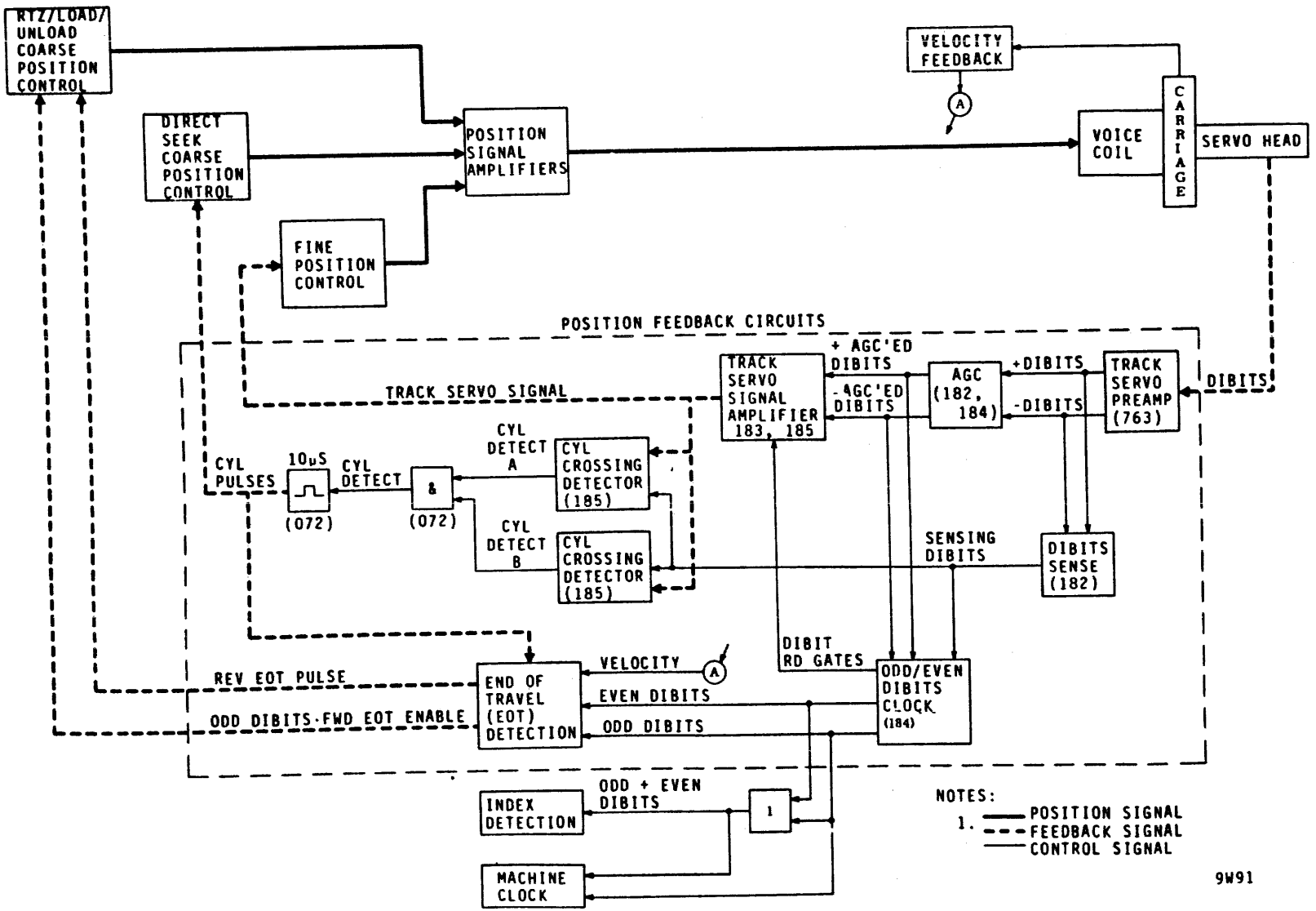


Figure 3-32. Position Feedback Circuits.

When the head is over the servo zone, it passes over both types of dibit tracks and the preamp produces a waveform that is a mixture of both types of dibit signals.

The amplitude of each dibit component in the waveform is proportional to how much the servo head is overlapping the tracks. If the head is centered over a servo track the signal has equal positive and negative dibit components. However, when the head is away from the centerline, the amplitude of one dibit component is greater than the other (this is shown on figure 3-33).

If the servo head is moving through the servo zone, each component alternately increases and decreases as the servo tracks are passed. This is also shown on figure 3-33.

The output of the track servo preamp is sent to the AGC and dibits detect circuit.

Dibit Sensing

The dibits sense circuit (refer to figure 3-32) detects the presence of dibits data. The output from this circuit is the Dibits Sense signal and it must be active (indicating dibits are present) for the position feedback circuits to function. This prevents them from generating false signals when no dibits are present (as for example, during a heads load or when heads are unloaded).

The Dibits Sense signal is first enabled during the heads load sequence when the heads loaded switch transfers. The signal goes active when dibits with an amplitude of at least 145 mv peak to peak have been present for 3 ms. If the Dibits Signal should drop below this level for more than 50 µs, the Dibits Sense signal goes inactive thus disabling the cylinder crossing, odd/even dibits clock and track servo amplifier circuits.

Therefore, losing dibits results in totally disabling the position feedback circuits.

Automatic Gain Control (AGC)

The purpose of the AGC circuits (refer to figure 3-32) is to provide gain control for the dibits signals before applying them to the track servo amplifier and odd/even dibits clock circuits. This gain control is necessary for proper servo system operation. The outputs from the AGC circuits are the AGC'ed Servo signals.

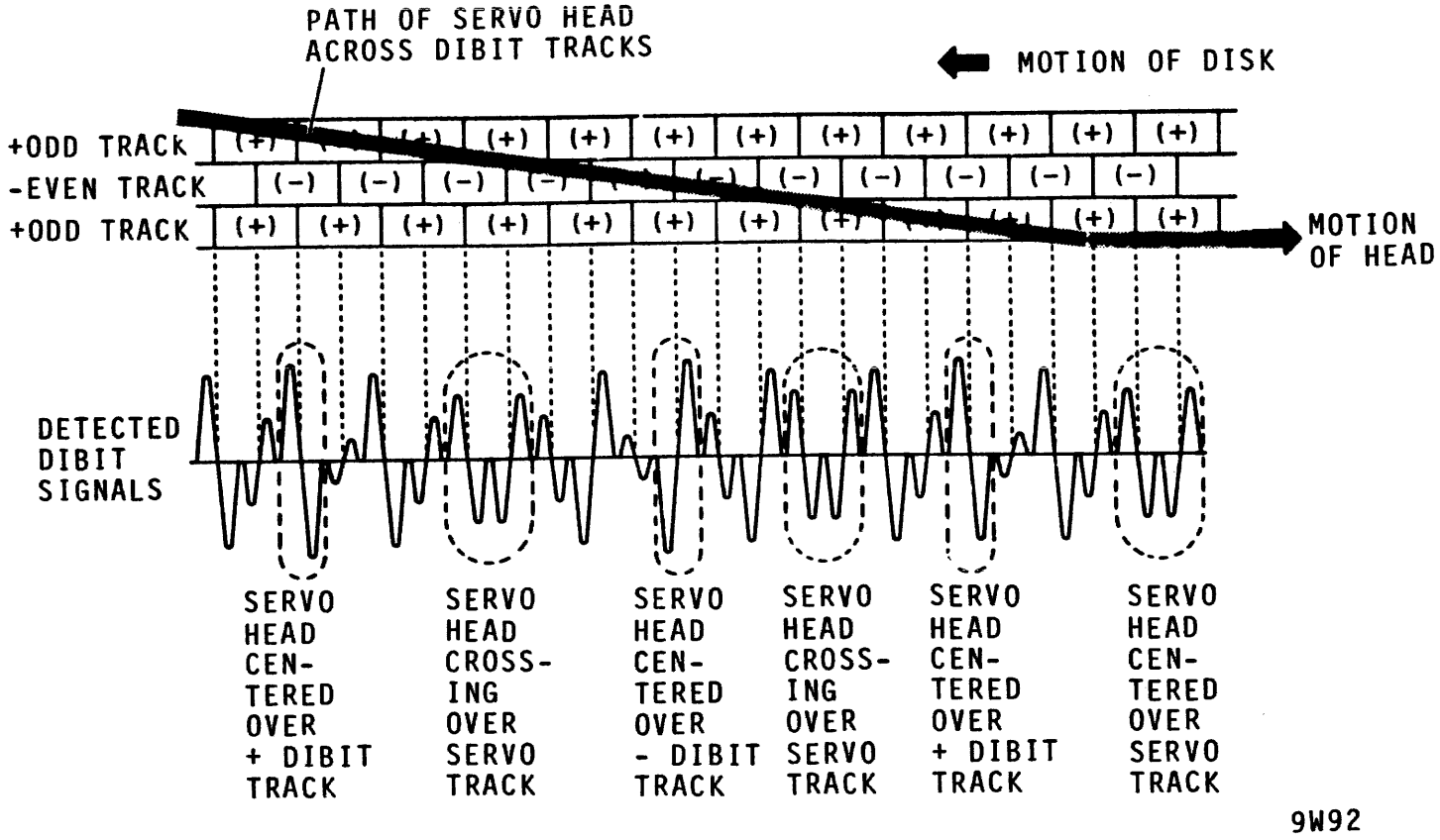


Figure 3-33. Servo Preamp Output

Gain control is obtained by feeding back a signal from the track servo circuit to the AGC circuits. This feedback signal, referred to as AGC, is derived from the AGC'ed Servo signals and the amplitude of the AGC and AGC'ed Servo signals are directly proportional. Therefore, when the AGC'ed Servo signals increase it causes an increase in the AGC signal and vice versa.

When the AGC signal increases, it causes a decrease in the gain of the AGC circuits. This results in reducing the amplitude of the AGC'ed Servo signal.

When the AGC signal decreases, the gain of the AGC circuits increases and the AGC'ed Servo signal becomes larger.

The net result is that the output amplitude of the AGC Circuit remains constant.

Track Servo Signal

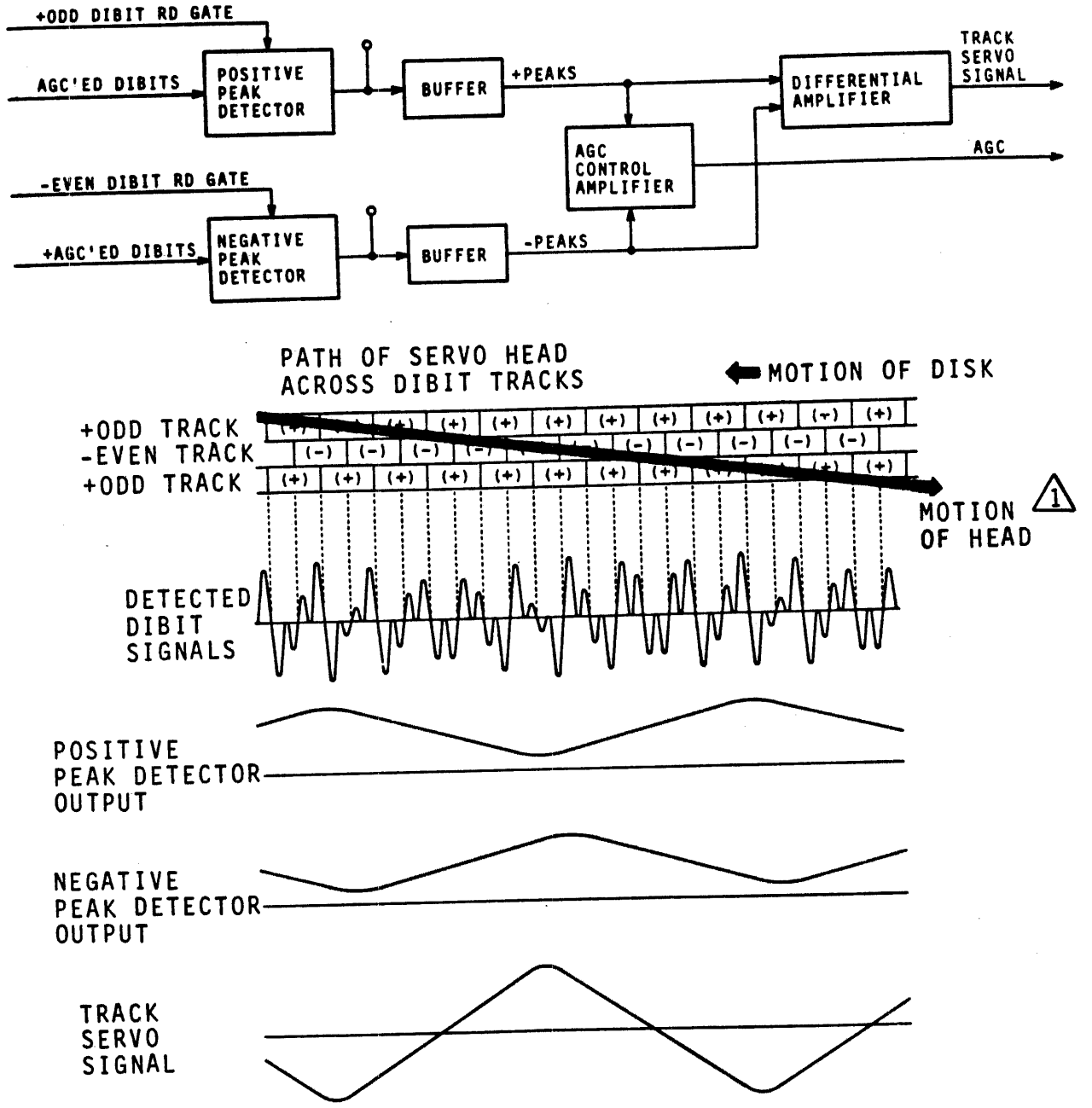
The track servo amplifier circuits (refer to figure 3-34) use the AGC'ed Servo signal from the AGC circuit and the Dibit read gate signals from the odd/even dibit clock circuits to produce a signal that varies as the position of the servo head changes with respect to the dibit tracks. This signal is referred to as the Track Servo signal.

The main elements in the track servo circuits are the peak detectors, peak detector buffers, AGC control amplifier and differential amplifier (refer to figure 3-34).

The peak detectors monitor the AGC'ed Dibits signals and are enabled by the Positive-Odd and Negative-Even Dibit Read Gate signals.

The positive peak detector is enabled by the Positive-Odd Dibit Read Gate signal and is active during the positive portion of the positive-odd dibit cycle. The negative peak detector is enabled by the Negative-Even Dibit Read Gate signal and is active during the negative portion of the negative-even dibit cycle. The peak detectors are inactive at all other times.

This results in peak detector outputs that are proportional to the amplitude of the dibit signals they are monitoring. Therefore, the positive peak detector output is maximum when the servo head is over a positive-odd dibit track and the negative peak detector output is maximum when the head is over a negative-odd dibit track (refer to figure 3-34).



NOTES:

1. MOTION OF HEAD EXAGGERATED.
2. ALL WAVEFORMS IDEALIZED FOR PURPOSES OF ILLUSTRATION.

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Figure 3-34. Track Servo Amplifier Circuit and Signals

The outputs of the peak detectors are processed by the peak detector buffers to provide signals of the proper amplitude and polarity for the AGC and differential amplifiers.

The AGC control amplifier uses the buffer outputs to generate the AGC voltage that is used by the AGC circuits.

The differential amplifier uses the two buffer outputs to produce a voltage with a polarity and magnitude directly proportional to the difference between them. This is the Track Servo signal.

The Track Servo signal is at its maximum positive value when the servo head is over negative-even dibit tracks and maximum negative when the servo head is over positive-odd dibit tracks.

If the servo head is centered over a servo track (between positive-odd and negative-even dibit tracks) the signal is zero. Therefore when the servo head moves through the servo zone, the Track Servo signal passes through zero each time the head crosses a servo track (refer to figure 3-34).

The Track Servo signal is applied to the Fine Position control and Cylinder crossing detection circuits. The Fine Position control circuits use the signal to generate the positioning signal that controls movement during the last one half track of a seek (and during forward EOT conditions). The Cylinder crossing detect circuits use the signal to generate cylinder pulses as each servo track is crossed.

Odd/Even Dibits Clock Generation

The odd/even dibits clock circuits (refer to figure 3-35) generate the Odd Dibits, Even Dibits and also the Odd and Even Dibits Read Clock signals. These signals are derived from the AGC'ed Dibits signals that are applied to the level detectors.

The level detectors create digital pulses from the AGC'ed Dibits signals by switching to their low state whenever they sense their respective dibit signals. The level detectors are enabled by the Sensing Dibits signal that is active only when dibits are being read from the disk.

The outputs from the level detectors produce both the Dibits Read gate and Odd/Even dibits signals.

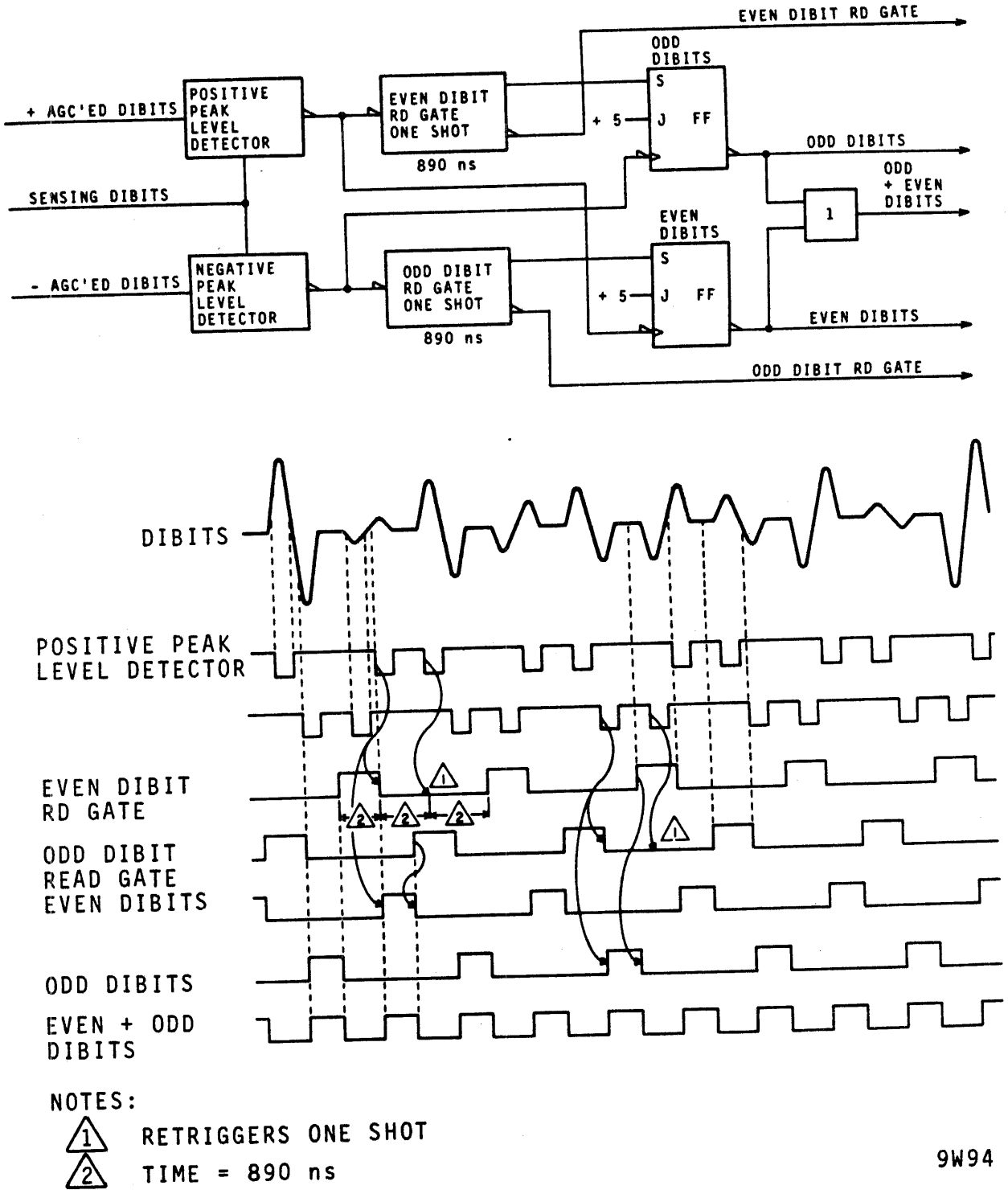


Figure 3-35. Odd/Even Dibit Clock - Logic and Timing

The Odd and Even Dibits Read Gate signals are generated when their respective one shots are triggered by the negative going edge of the level detector outputs. The dibit read gate signals enable the track servo amplifier circuits.

The Odd Dibits and Even Dibits signals are produced by the outputs of the level detectors working in conjunction with the output of the dibits read gate one-shots. The logic and timing for this is shown on figure 3-35.

The Odd Dibits and Even Dibits signals have a nominal frequency of 403 kHz. However, because they are in turn derived from dibits that are derived from the rotating disk, this frequency will vary with disk speed.

The Odd or Even Dibits signal is generated by ORing the Odd Dibits and Even Dibits signals. This produces an 806 kHz (nominal) signal that also varies with disk speed.

The Odd Dibits, Even Dibits and Odd or Even Dibits signals are used by the machine clock, index detection and End of Travel Detection circuits (refer to discussion on these circuits for more information).

Cylinder Crossing Detection

The cylinder crossing detection circuits (refer to figure 1-15) use the Track Servo signal to generate a pulse as each servo track is crossed.

When the servo head crosses a servo track, the heads are crossing a cylinder (refer to discussion on Cylinder Concept); therefore, these pulses are called Cylinder Pulses.

The cylinder crossings are detected by cylinder crossing detectors A and B. Cylinder crossing detector A produces an output pulse from the time the Track Servo signal goes through zero in a positive direction until it goes through -0.4 V in a negative direction . Cylinder crossing detector B produces an output pulse from the time the Track Servo signal goes through zero in a negative direction until it goes through +0.4 V in a positive direction.

This results in an overlapping of the two pulses after each zero crossing (refer to figure 3-36) and combining them produces a pulse to trigger the 40 microsecond 10 microsecond Cylinder Pulse one shot.

The 10 microsecond Cylinder Pulses from the one shot are used by the direct seek coarse control circuits to count the number of cylinders crossed during a seek. They are also used by the End of Travel Detection circuits. Refer to the discussions on these circuits for further descriptions of how they are used.

It should be noted that the cylinder crossing detection circuits are operative only when the heads are loaded and dibits are being read from the disk. At all other times, the Sensing Dibits signal is inactive thus disabling the cylinder crossing detectors. This prevents false Cylinder Pulses from being generated.

End of Travel Detection

The end of travel (EOT) detection logic (refer to figure 3-37) senses when the heads are outside of the data area and over one of the guard bands. Depending on the type of seek being performed, the output from this circuit will be interpreted as either an error indication or a feedback signal.

If the drive is performing a direct seek to one of the tracks in the data area, an EOT is interpreted as a positioning error and the proper error sequence is initiated. However if an RTZ or Load seek is being performed, the EOT signals are used as feedback for the RTZ/Load coarse position control circuits.

The main elements in the EOT detection circuits are the EOT Integrator, EOT detectors and the Forward and Reverse EOT FFs.

The EOT Velocity Integrator works similarly to the Desired Velocity Integrator in the direct seek coarse position control circuits. It monitors the Velocity signal and generates a sawtooth output waveform that rises from zero until reset by either a Cylinder pulse (when moving through data area) or by the Reverse EOT Pulse (during an RTZ when it detects the reverse EOT). If neither of these are present (as when moving over the outer or inner guard band), the output continues to rise.

The output from the EOT Velocity Integrator is monitored by the Forward and Reverse EOT detectors. The Forward EOT Detector is enabled whenever the integrator output exceeds +1.35 volts. This occurs either during a load when the heads are moving forward through the inner guard band or whenever the heads move into the outer guard band. In both of these cases the Velocity signal is of the proper polarity, and there are no pulses to reset the integrator.

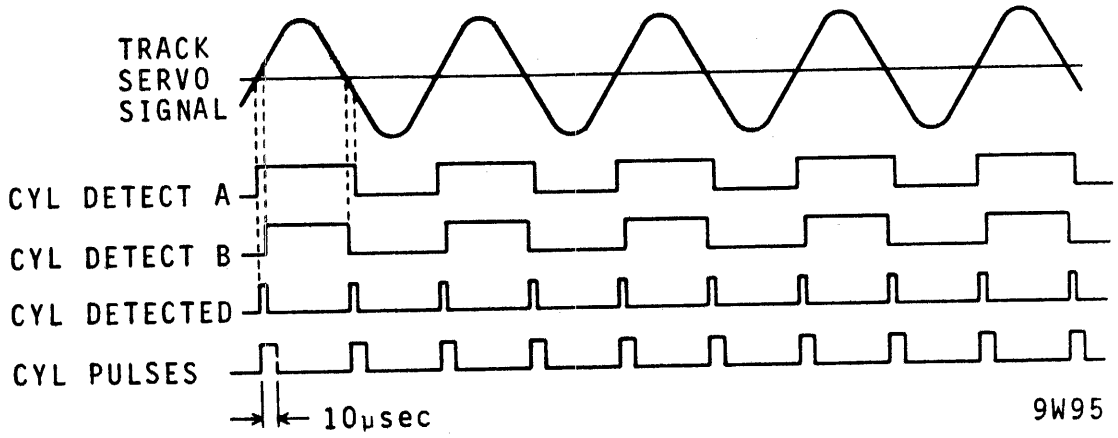


Figure 3-36. Cylinder Crossing Detection

The Reverse EOT Detector is enabled whenever the Integrator output is more negative than -1.35 volts. This occurs when the heads are moving in reverse over the outer guard band.

The Forward and Reverse EOT Enables are applied to the Forward and Reverse EOT FFs. The conditions causing these FFs to set and clear are shown on figure 3-37

VELOCITY FEEDBACK GENERATION

The velocity of the carriage must be controlled to have the shortest seek time without having the heads overshooting or oscillating around the desired cylinder. The signal to provide this control is generated by the velocity feedback circuits (refer to figure 3-38).

The velocity of the carriage is sensed by the velocity transducer. This is mounted within the magnet and consists of a stationary coil and movable magnetic core (refer to figure 3-38).

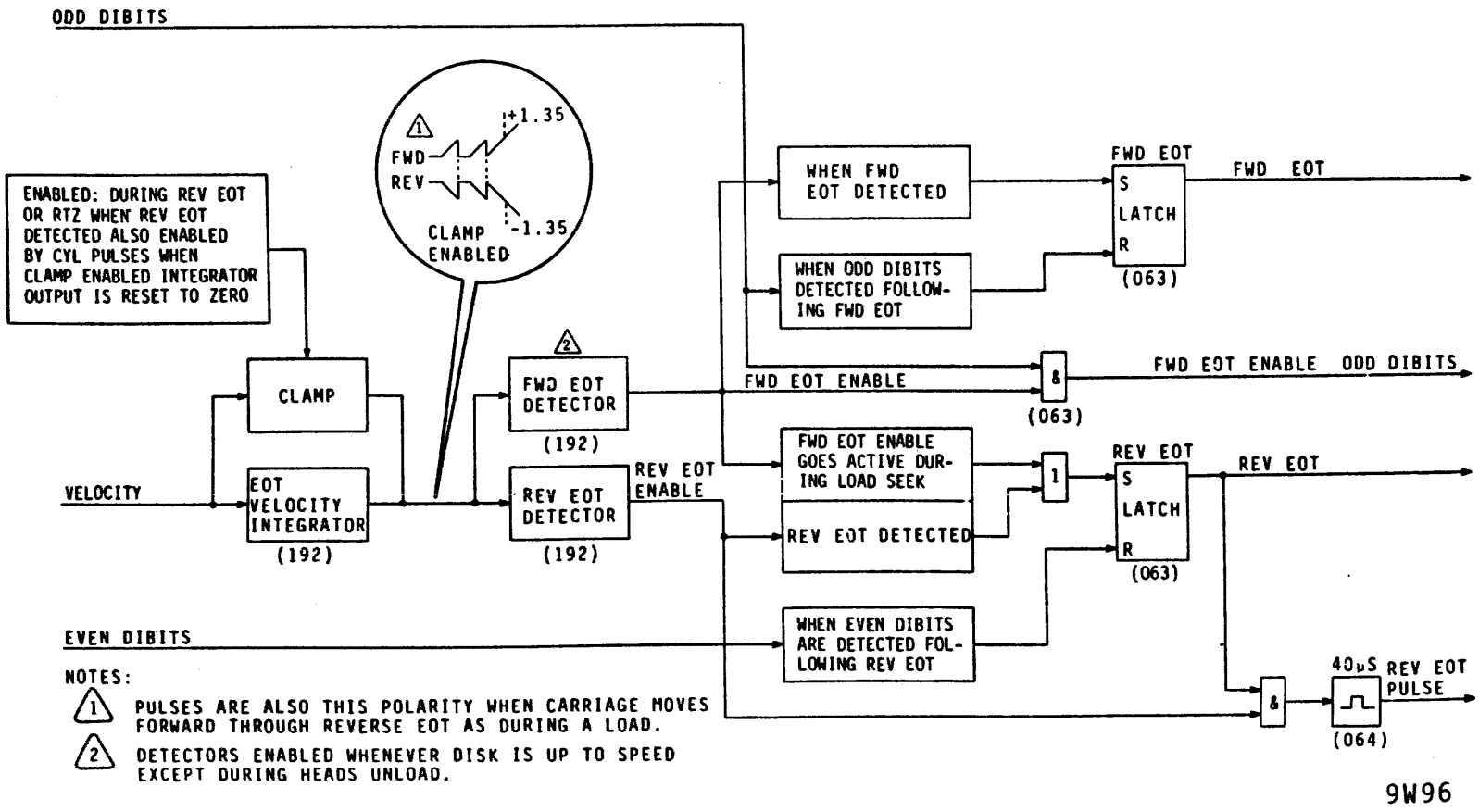


Figure 3-37. End of Travel Detection Circuits

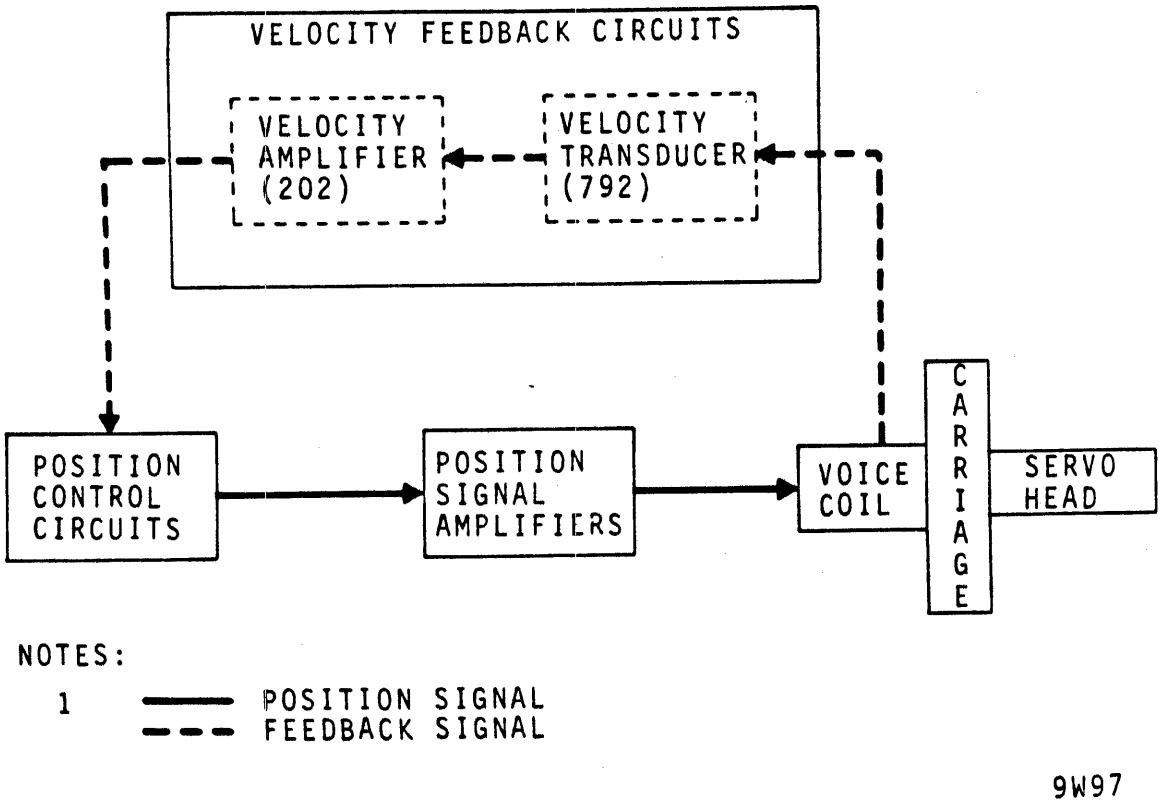


Figure 3-38. Velocity Feedback Circuits

When the carriage moves, the core moves thus inducing an EMF in the coil. This EMF is converted by the velocity amplifier into the velocity signal.

The amplitude of this signal varies with the speed of the carriage and the polarity depends on the direction of movement. If the seek is in a forward direction, the polarity is negative, and if it is in a reverse direction, the polarity is positive.

Refer to the discussion on Electromechanical Functions for further description of the velocity transducer.

POSITION SIGNAL AMPLIFICATION

The signals from the position control circuits are processed by the position amplifier circuits (refer to figure 3-39) to provide the current for the voice coil.

Any one of the three position signals may provide the input to these circuits depending on the type of seek being performed and how close the heads are to the destination. This input signal is applied to the summing amplifier.

The output from the summing amplifier is then applied to the power amplifier driver, which uses it to generate the Forward and Reverse Current signals. These signals are sent to the power amplifier.

The power amplifier uses the Forward and Reverse Current signals to produce a voice coil current with the proper polarity and amplitude to move the voice coil and carriage thereby positioning the heads.

DIRECT SEEK POSITION CONTROL

General

A direct seek is one in which the drive is commanded by the controller to move the heads from their current logical cylinder location to another, specified by the controller. The controller initiates the direct seek via Cylinder Select Tag 1 and Bus Bits 0-9.

The direct seek function is divided into two modes: (1) coarse and (2) fine. The coarse mode consists of all but the last half track of the seek. The servo system is in fine mode during the last half track and while the heads are tracking over the desired cylinder.

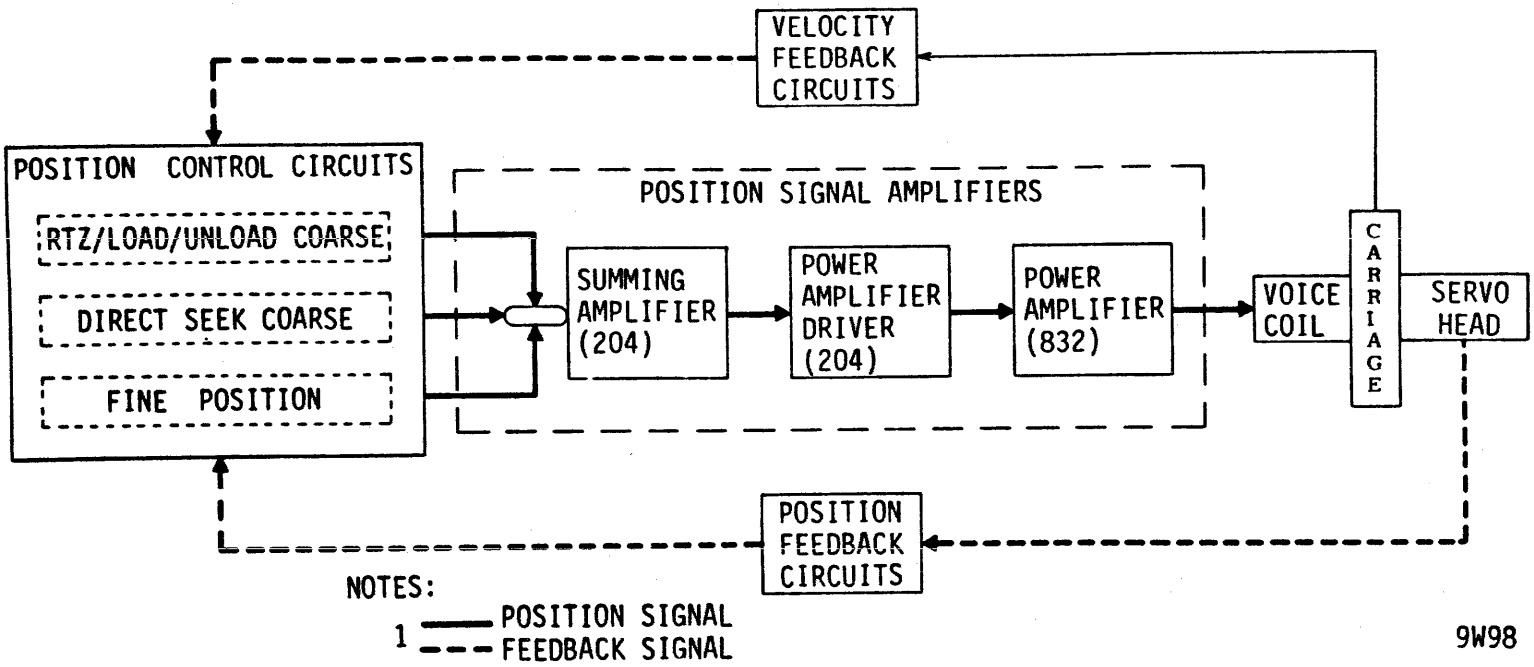


Figure 3-39. Position Signal Amplifier Circuits

The following discussions describe both the coarse and fine modes. Figure 3-40 is a flow chart of the entire direct seek function.

Direct Seek Coarse Control

General

The direct seek is controlled by the direct seek coarse control circuits for all but the last half track of the seek. Figure 3-41 shows these circuits and the signals they generate.

The three main inputs to these circuits are the address of the destination cylinder (received from the controller in conjunction with the cylinder address tag), the Cylinder pulses (received from the position feedback circuits), and the Velocity signal (received from the velocity feedback circuits). These signals are used to produce a coarse positioning signal that varies with distance and also controls the speed of the carriage as it moves toward the destination.

How the coarse positioning signal is generated and also how the loop operates under coarse control is explained in the following paragraphs.

Coarse Position Signal Generation

At the start of the seek, the distance to the destination cylinder is determined by the adder. It does this by comparing the address sent by the controller with the address presently contained in the cylinder address register (this is the address at which the heads are presently located) and then generating a difference count indicating how many logical cylinders the heads will have to cross in reaching the new address.

The difference count is loaded into the Difference counter. After the difference counter is loaded, the new address (received from the controller) is loaded into the Cylinder Address register and will be the present address at the start of the next seek.

The Difference counter is decremented by the cylinder pulses as each logical cylinder is crossed thus keeping track of the number of logical cylinders left in the seek.

The seven lower order bits of the Difference counter go to the D/A converter, as shown in figure 3-41.

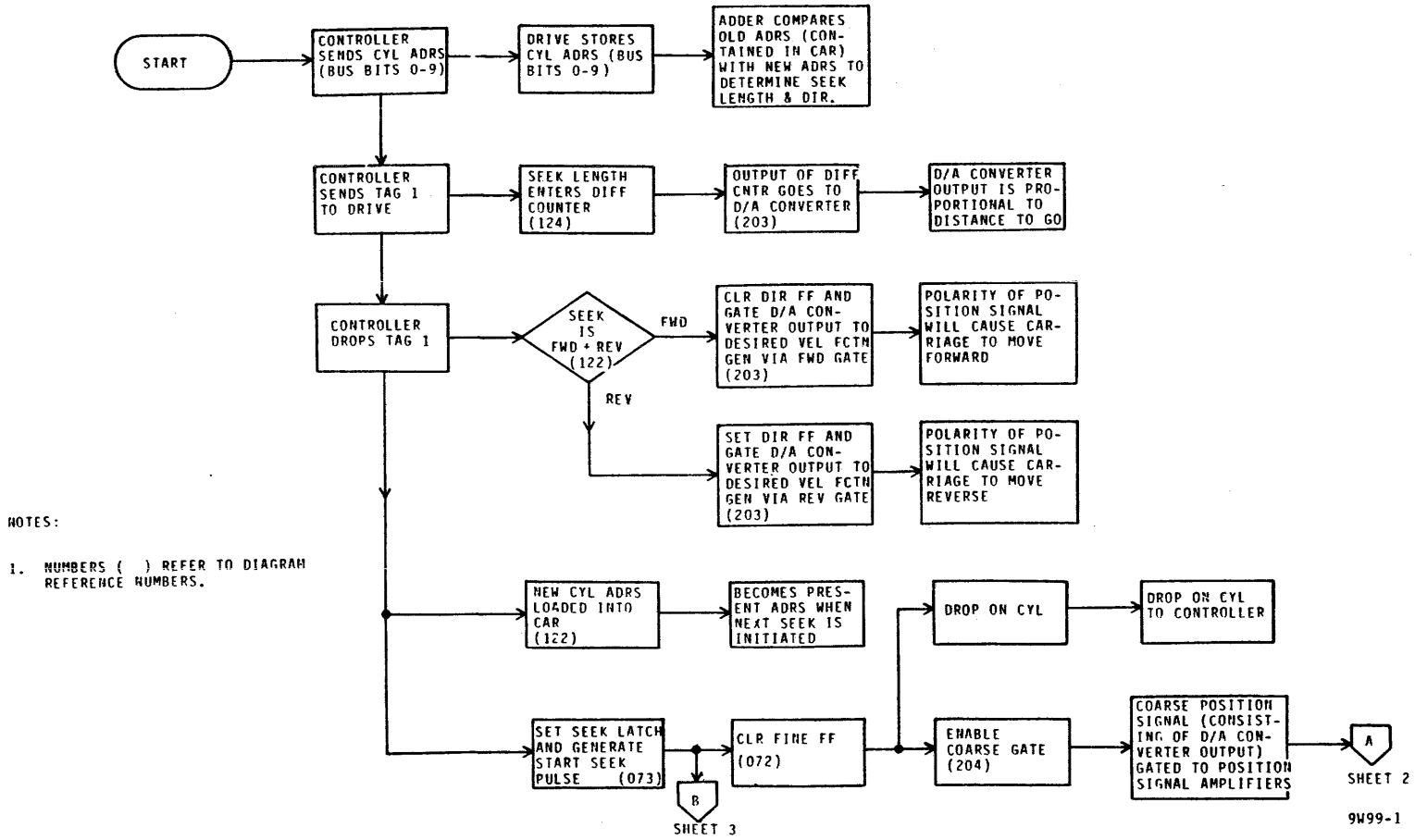


Figure 3-40. Direct Seek Flow Chart (Sheet 1 of 3)

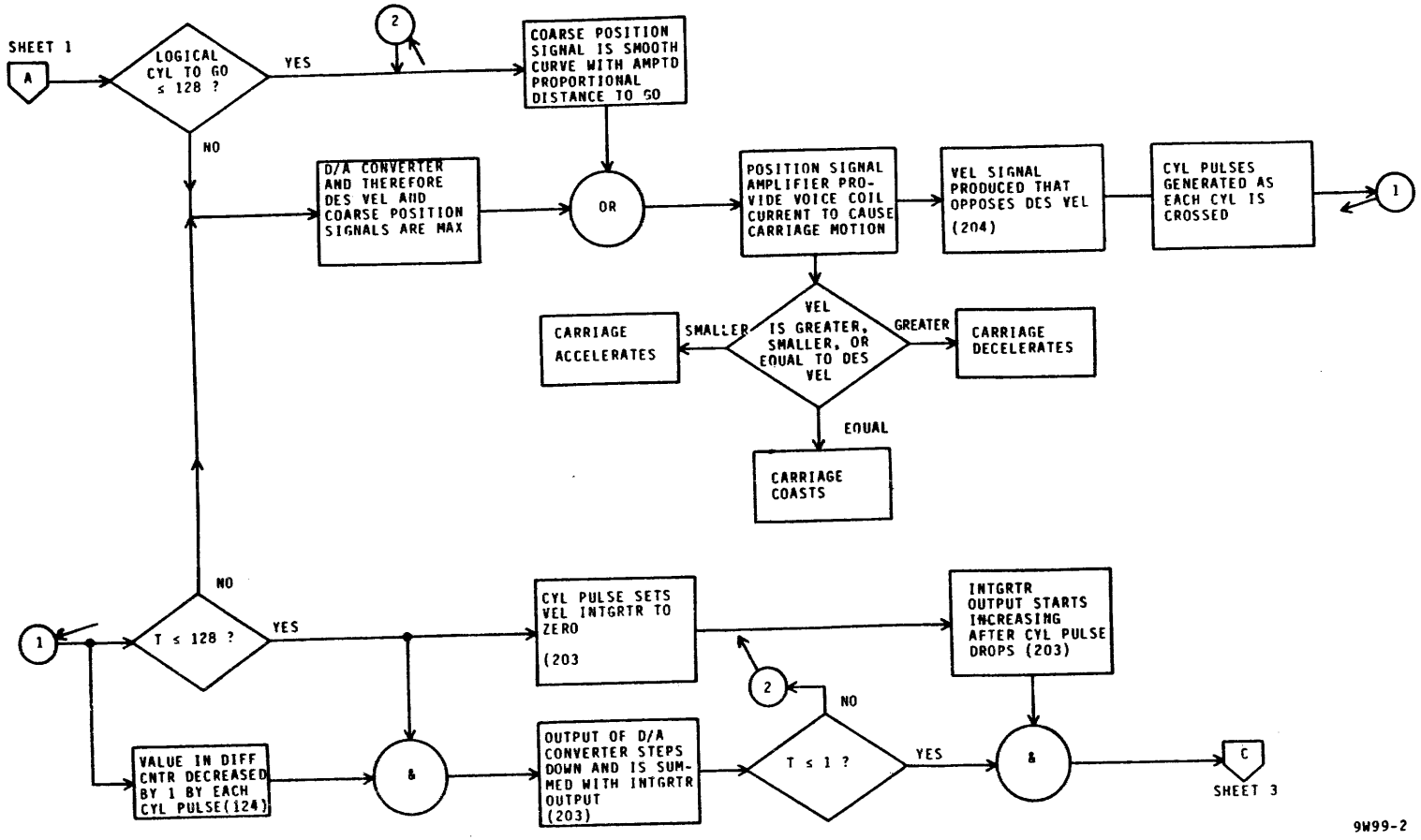


Figure 3-40. Direct Seek Flow Chart (Sheet 2)

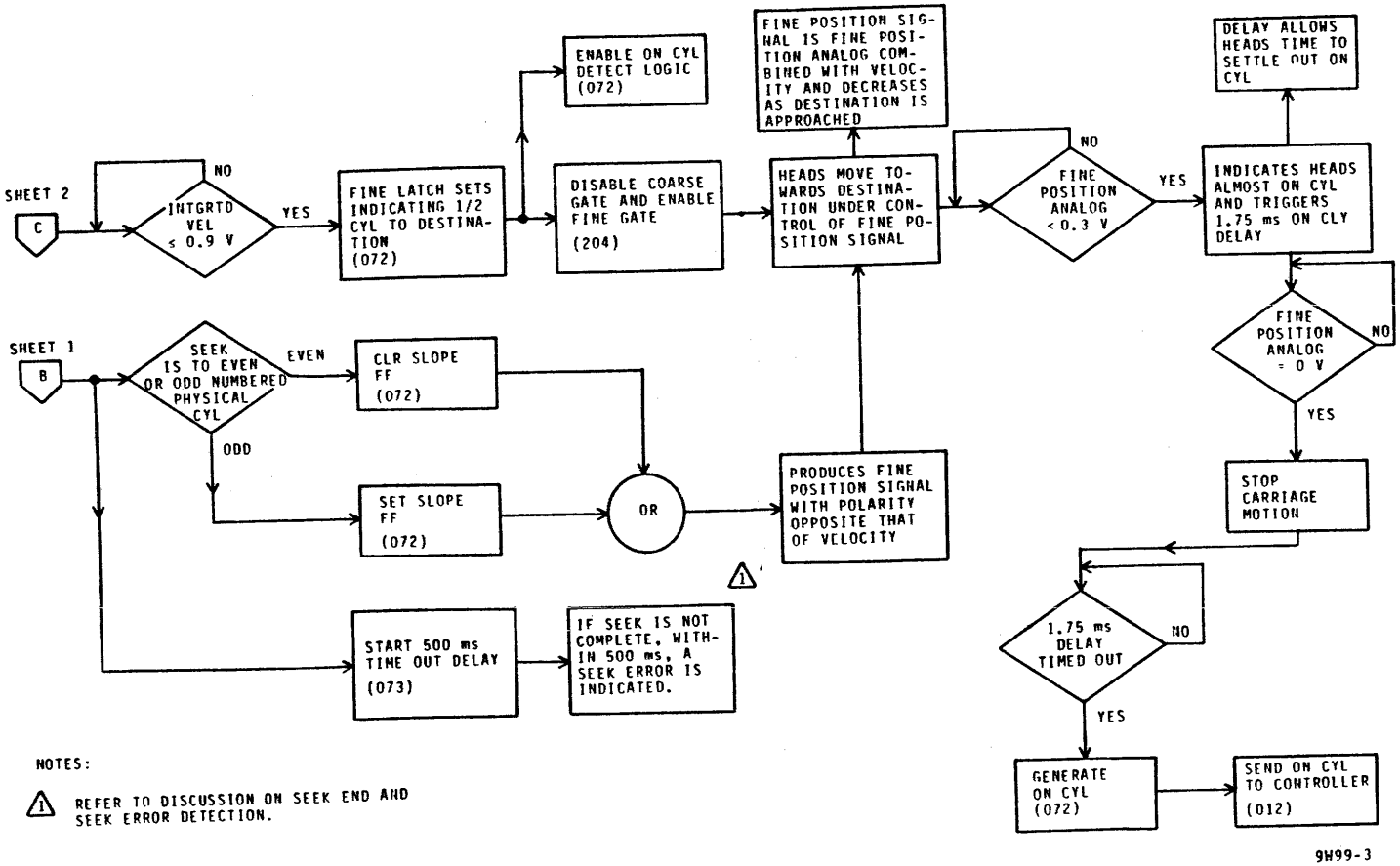


Figure 3-40. Direct Seek Flow Chart (Sheet 3)

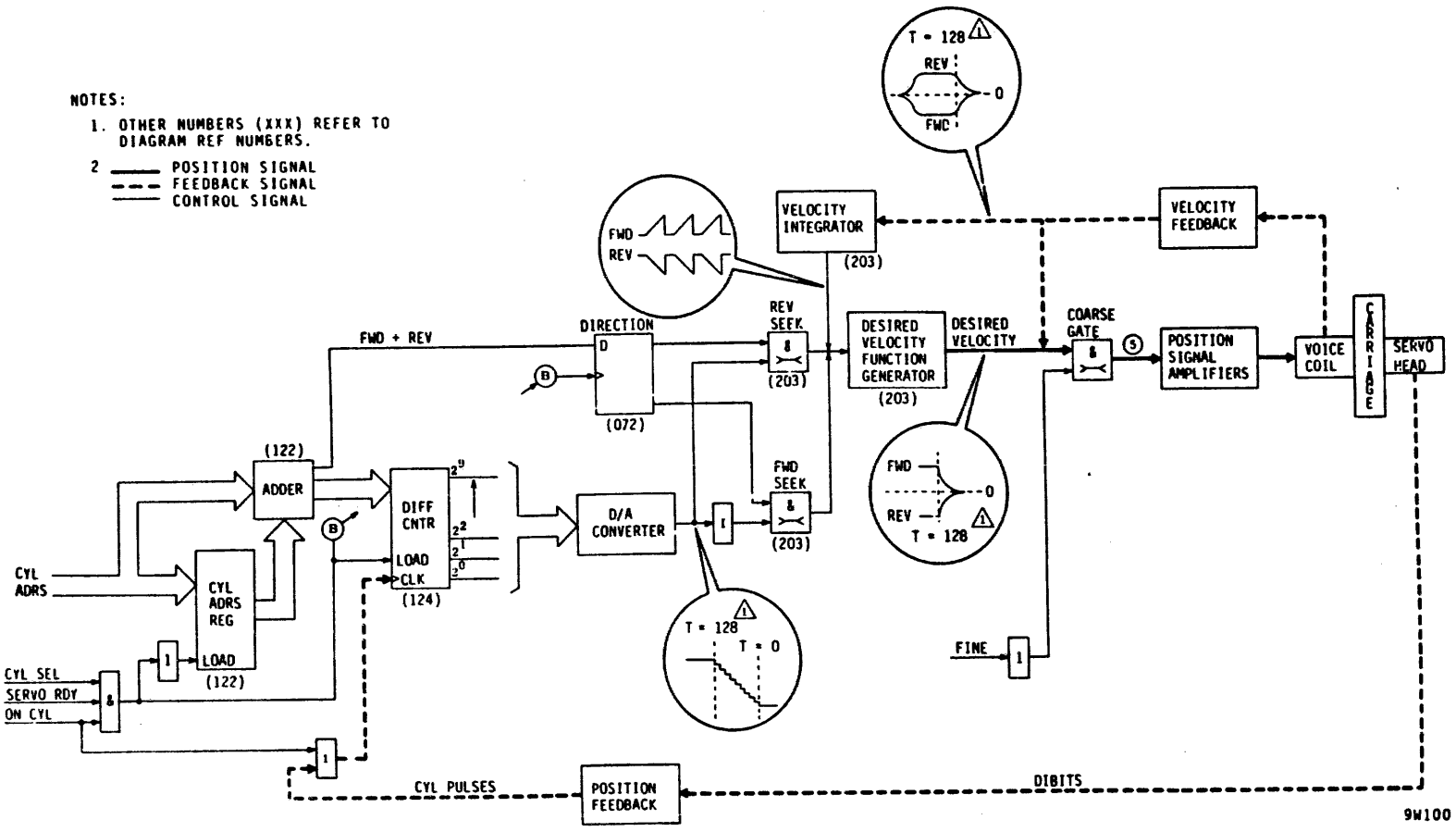


Figure 3-41. Direct Seek Coarse Position Control Circuits

The output of the D/A converter is determined by the value of the input bits from the Difference counter. When these bits are all active, the D/A Converter output is maximum. This is the case where the number of logical cylinders to go exceeds 128. However, when logical cylinders to go are less than 128, the D/A Converter output steps down (with the counter output) as each logical cylinder is crossed.

The D/A Converter output signal is gated via either the Forward or Reverse gate to the Desired Velocity Function Generator. The output of the Desired Velocity Function Generator (Desired Velocity) varies in amplitude with the D/A Converter output (and therefore with distance to the destination) and in polarity depends upon the direction of the seek.

The seek direction is determined at the start of the seek by the adder, which generates the Forward or Reverse signal. This signal either sets or clears the Direction FF and thereby enables either the Forward or Reverse Gate.

If the seek is in a forward direction (toward the spindle), the Direction FF is cleared thus enabling the Forward gate. This causes a Desired Velocity signal that varies from a negative voltage to zero.

If the seek is in a reverse direction (away from the spindle), the Direction FF is set thus enabling the Reverse gate. In this case, the Desired Velocity signal varies from a positive voltage to zero.

In either case, the output from the D/A Converter must be smoothed out during the last 128 logical cylinders of a seek to prevent steps from appearing in the Desired Velocity output. This function is performed by the Velocity Integrator.

The Velocity Integrator is enabled when logical cylinders to go reaches 128 and at this point starts generating sawtooth pulses. These pulses start from zero at the time the Cylinder pulse goes false (which occurs after the cylinder crossing) and rise until by the next cylinder pulse (which occurs at the next cylinder crossing).

When the sawtooth pulses are summed with the D/A Converter output, the resulting Desired Velocity signal is a smooth curve that decreases in amplitude with distance to the destination cylinder.

The Desired Velocity signal is then summed with the Velocity signal received from the velocity feedback circuits. The Velocity signal varies in amplitude with carriage speed and is opposite in polarity to the Desired Velocity signal. It is necessary to sum Desired Velocity with Velocity in order to control carriage speed thus ensuring minimum seek time without overshooting the destination cylinder.

The resultant signal, Desired Velocity summed with Velocity, is the final output of the coarse position circuits and is applied to the position signal amplifiers via the coarse gate.

Loop Operation During Coarse Control

The position signal amplifiers use the output from the coarse position amplifier circuits to produce current for the voice coil. This current controls carriage motion.

The Coarse control portion of a typical direct seek can be divided into three phases:

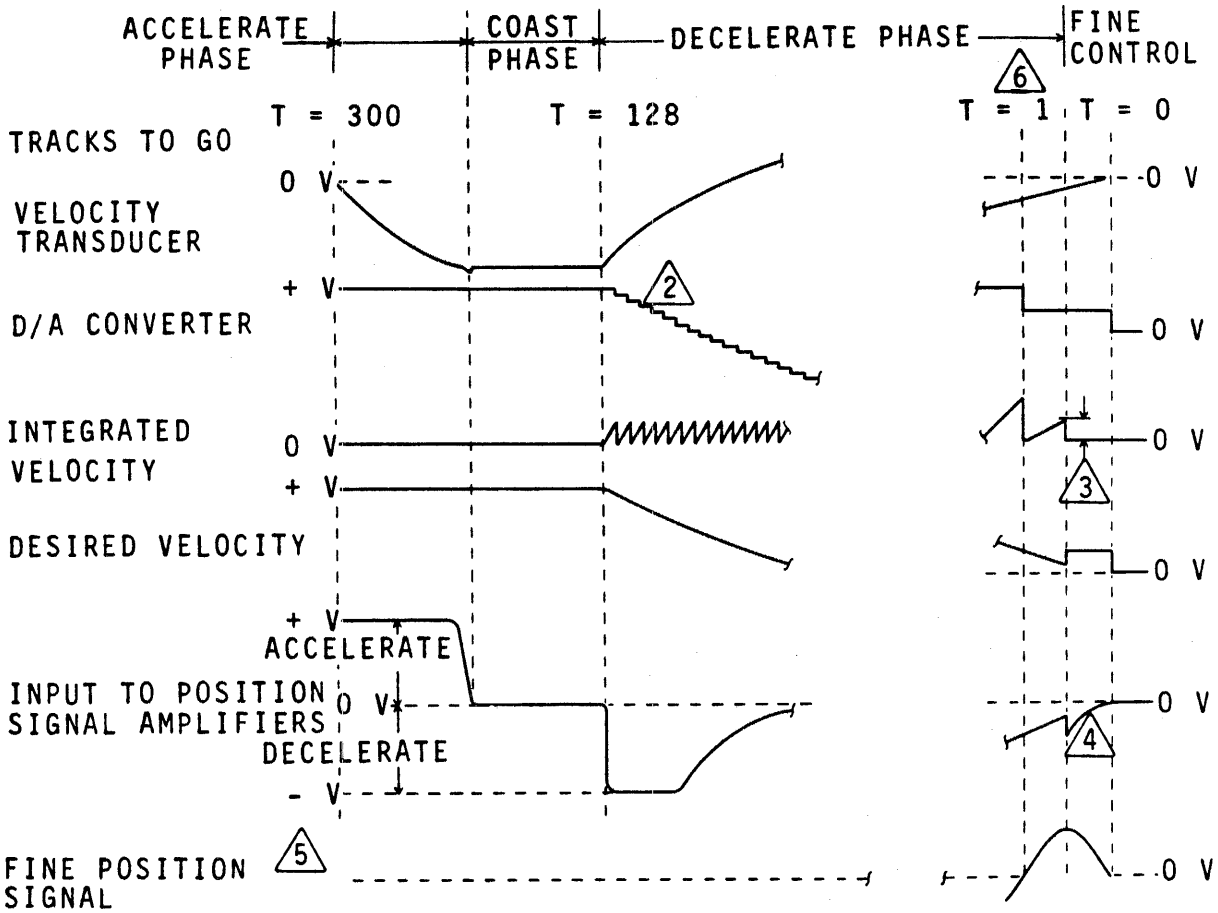
- Accelerate Phase - Voice coil receives maximum current and carriage accelerates from zero to maximum velocity.
- Coast Phase - Carriage is at maximum velocity and coasts along under its own inertia.
- Deceleration Phase - Carriage approaches destination and must slow down to avoid overshoot.

It should be noted that it takes about 60 cylinders for the carriage to reach maximum velocity (about 55 in/s). During shorter seeks, particularly those less than 128 logical cylinders, maximum velocity will not be obtained. In cases where maximum velocity is not reached, the primary functions remain the same but the coast phase will not occur (or be very short), and the carriage begins to decelerate sooner.

The following describes how the servo loop operates during a typical direct seek long enough for the drive to obtain maximum velocity. The signals generated are shown in figure 3-42.

The acceleration phase occurs during the first part of the seek. At this time, the carriage is stationary and the output from the coarse gate is due entirely to the Desired Velocity signal with no opposing Velocity signal. Therefore, voice coil current is maximum in the direction necessary to cause maximum carriage acceleration.

As the carriage accelerates, a Velocity signal is generated by the velocity feedback circuits. Because this signal opposes the Desired Velocity signal, the resultant signal to the position signal amplifiers is reduced thereby reducing voice coil current. However, Desired Velocity signal is still greater and the carriage continues to accelerate.



NOTES:

1. SIGNALS SHOWN APPLY TO FWD SEEK ABOUT 300 CYL IN LENGTH, ALL POLARITIES EXCEPT D/A CONVERTER ARE OPPOSITE FOR REV SEEKS. TIMING AND AMPLITUDE ARE NOT TO SCALE.

2. OUTPUT DECREASES WITH EACH CYLINDER PULSE.

3. SERVO SYSTEM SWITCHES TO FINE CONTROL WHEN INTEGRATED VELOCITY EXCEEDS 0.9 V.

4. GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. SIGNAL FOR LAST HALF TRACK IS DUE TO FINE POSITION INPUT AND IS SHOWN HERE FOR REFERENCE ONLY.

5. FROM FINE POSITION CONTROL CIRCUITS AND IS SHOWN FOR REFERENCE ONLY.

6. SCALE EXPANDED FOR CLARITY BEYOND T = 1. 9W101

Figure 3-42. Direct Seek Coarse Position Control Signals

Eventually carriage speed increases to the point where the Velocity signal equals the Desired Velocity signal and the two signals cancel one another. This causes the positioning signal from the coarse gate, and therefore the voice coil current, to drop to zero. The carriage now coasts along at a maximum velocity of about 55 in/s.

As the carriage coasts, friction losses and back EMF of the moving voice coil tend to slow it down. However, when this occurs, the velocity signal becomes less than the Desired Velocity signal (which is still maximum) thus causing enough voice coil current to speed up the carriage until the two signals cancel again.

This continues as long as the Desired Velocity signal remains at its maximum value, which is until less than 128 cylinders remain in the seek. Beyond this point, the carriage starts to decelerate.

When less than 128 cylinders remain, the D/A Converter starts to step down thus causing the Desired Velocity signal to decrease.When Desired Velocity is less than Velocity, current is applied to the voice coil in the reverse direction causing the carriage to slow down until the Velocity signal is again equal to Desired Velocity. The carriage now coasts under its own inertia until the D/A Converter steps down again.

This process continues and the carriage slows down as the destination cylinder is approached. When the heads are within one half track of the destination, the servo system switches to fine control.

Direct Seek Fine Control

General

The last half track of a direct seek is controlled by the fine position control circuits (refer to figure 3-43). These circuits generate the signal used to bring the drive over the desired cylinder and to keep it tracking properly over this cylinder.

In addition to this, these circuits also control coarse to fine switching and generate the On Cylinder signal. The following paragraphs describe all of these functions and is divided into these areas:

- Coarse to Fine Switching
- Fine Position Signal Generation

- On Cylinder Detection
- Track Following

Figure 3-43 shows the fine position control circuits and figure 3-44 shows timing during fine position control.

Coarse to Fine Switching

Coarse to fine switching is controlled by the Fine latch. When this latch is set, the Fine gate is enabled and the output of the fine position control circuit gates to the position signal amplifiers. Whenever this latch is cleared, the coarse gate is enabled thus putting the servo system in coarse control.

During a direct seek, the Fine latch clears at the start of the seek and remains clear until the heads are within one half cylinder of destination.

The coarse to fine sequence starts when the Difference counter indicates one cylinder to go. At this time the $T \leq 1$ signal goes active indicating the last cylinder is being crossed.

The one half cylinder point is sensed by the fine control level detect circuit. The input to this circuit is the Integrated Velocity signal (refer to discussion on Direct Seek Coarse Control), which is set to zero by the same cylinder pulse that decrements the Difference counter to one. When this cylinder pulse drops, the Velocity Integrator output starts to increase again. When it reaches 0.9 V, the heads are about one half cylinder from the centerline of the destination cylinder and this causes the fine control level detect output to go active. This causes the Fine Enable signal to go active. The Fine Enable signal is then ANDed with the $T \leq 1$ signal to set the Fine latch.

When the Fine latch sets, the coarse gate is disabled and the Fine gate is enabled thus gating the fine positioning signal to the position signal amplifiers.

Fine Position Signal Generation

The fine positioning signal is produced by combining the Fine Position Analog and Velocity signals. The Fine Position Analog signal varies with distance to the destination cylinder centerline and Velocity varies with speed of the carriage.

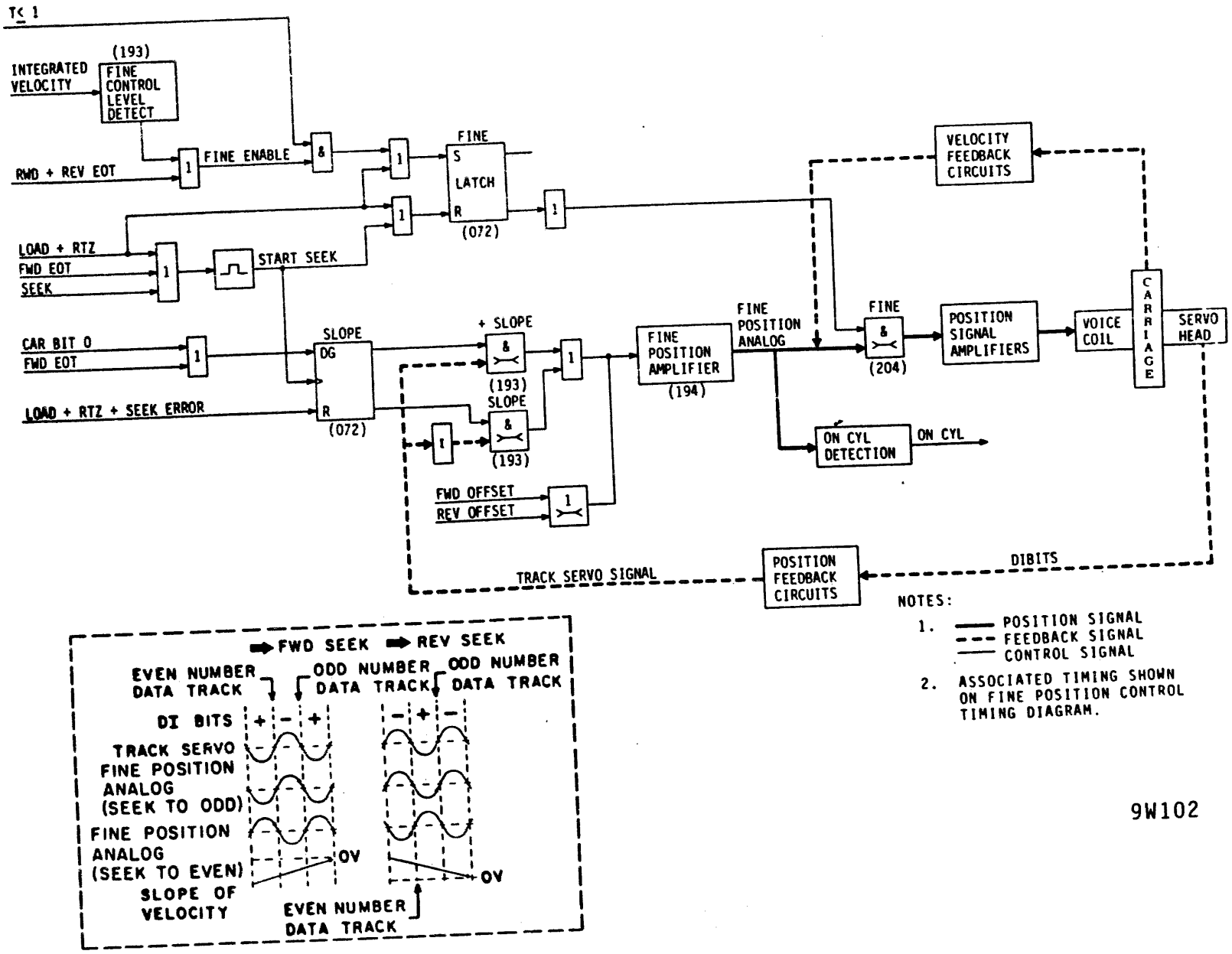
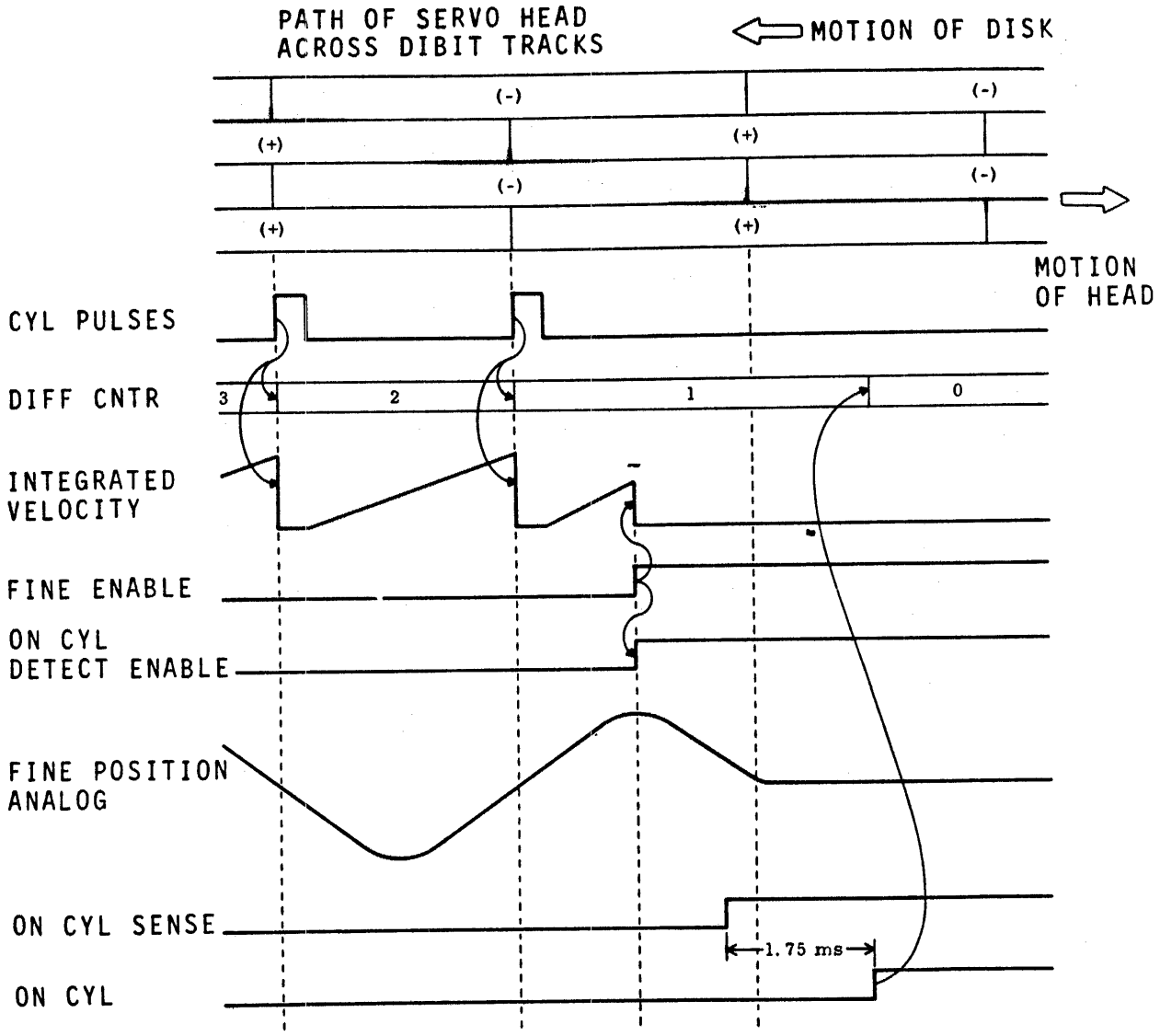


Figure 3-43. Fine Position Control Circuits



NOTES:

1. REFER TO FIGURES SHOWING FINE POSITION CONTROL AND ON CYL DETECTION CIRCUITS FOR LOGIC ASSOCIATED WITH THIS TIMING.

9W103

Figure 3-44. Fine Position Control Timing

The Fine Position Analog signal is derived from the Track servo signal that is received from the position feedback circuits and provides the position feedback during fine control. The amplitude of the Fine Position Analog and Track Servo signals are directly proportional and as the heads approach the centerline of the destination cylinder both signals decrease from maximum to zero.

The Fine Position Analog signal is summed with the Velocity signal to provide speed control. These signals are of opposite polarity with the polarity of Fine Position Analog such as to cause an increase in carriage speed and the polarity of Velocity such as to cause a decrease.

Because, during this phase, the carriage must decelerate, the amplitude of the Velocity signal will normally be greater than that of Fine Position Analog. How much greater depends on the speed of the carriage.

If the carriage starts moving too fast, the Velocity signal will increase and therefore exceed Fine Position Analog by a greater amount. This results in greater deceleration. However, if the carriage decelerates too quickly the Velocity signal decreases and approaches that of Fine Position Analog resulting in less deceleration.

Ideal speed is obtained when the two signals are nearly equal and the resultant signal produces a voice coil current that brings the heads to rest at the destination cylinder without overshoot or oscillation.

Because the polarities of the Velocity and Fine Position Analog signals must be opposite, it is sometimes necessary to invert the Track Servo signal to obtain the proper polarity of Fine Position Analog. This is the case, because although the Velocity signal always has the same polarity (negative for forward seeks, positive for reverse seeks), the polarity of the Track Servo signal depends on whether it is approaching an odd or even numbered physical cylinder. On forward seeks, the Track Servo signal decreases from a maximum positive to zero when approaching an odd cylinder and increases from a maximum negative to zero when approaching an even cylinder. The opposite is true for reverse seeks. Refer to discussion on position feedback for more information on Track Servo signal generation.

What polarity the Fine Position Analog signal, which is derived from the Track Servo signal, will have is controlled by the Slope FF. This FF is either set or cleared at the start of the seek.

If the seek is to an odd numbered cylinder, the FF is set and the Fine Position Analog and Track Servo signals are of the same polarity. If the seek is to an even numbered cylinder, the FF is cleared and the signals are of opposite polarities. The phase relationships between the Track Servo and Fine Position Analog signals are shown on figure 3-43.

When the heads are centered over and tracking over the destination cylinder, both the Fine Position Analog and Velocity signals are zero. When this occurs the heads are considered to be on cylinder. This condition is sensed by the on cylinder detection circuits.

On Cylinder Detection

On cylinder detection is enabled when the servo system goes into fine control (Fine latch sets). At this time, the on cylinder detection circuits (refer to figure 3-45) start to monitor the Fine Position Analog signal. When this signal is small enough to indicate the heads are approximately over the servo track (if the destination cylinder), Cylinder Detect A and B signals go active thus enabling the On Cylinder Sense signal. The On Cylinder Sense signal triggers the 1.75 ms On Cylinder Delay, which allows the heads time to settle out over the servo track. When the delay times out, the On Cylinder FF sets.

The On Cylinder signal causes the On Cylinder line to the controller to go active and is also used to perform various functions within the drive logic.

Track Following

Even after the on cylinder position is obtained, it is necessary to keep the servo system under control of the fine position control circuits. This is necessary to ensure that the heads do not drift far enough off the track centerline to cause errors during a read or write operation.

If the heads should drift off centerline, the Track Servo signal will increase or decrease slightly from zero (depending on the direction of the drift) and this is translated into the Fine Position Analog signal. The polarity of the Fine Position Analog is such that the position signal amplifier generates the proper voice coil current to drive the heads back to the track centerline.

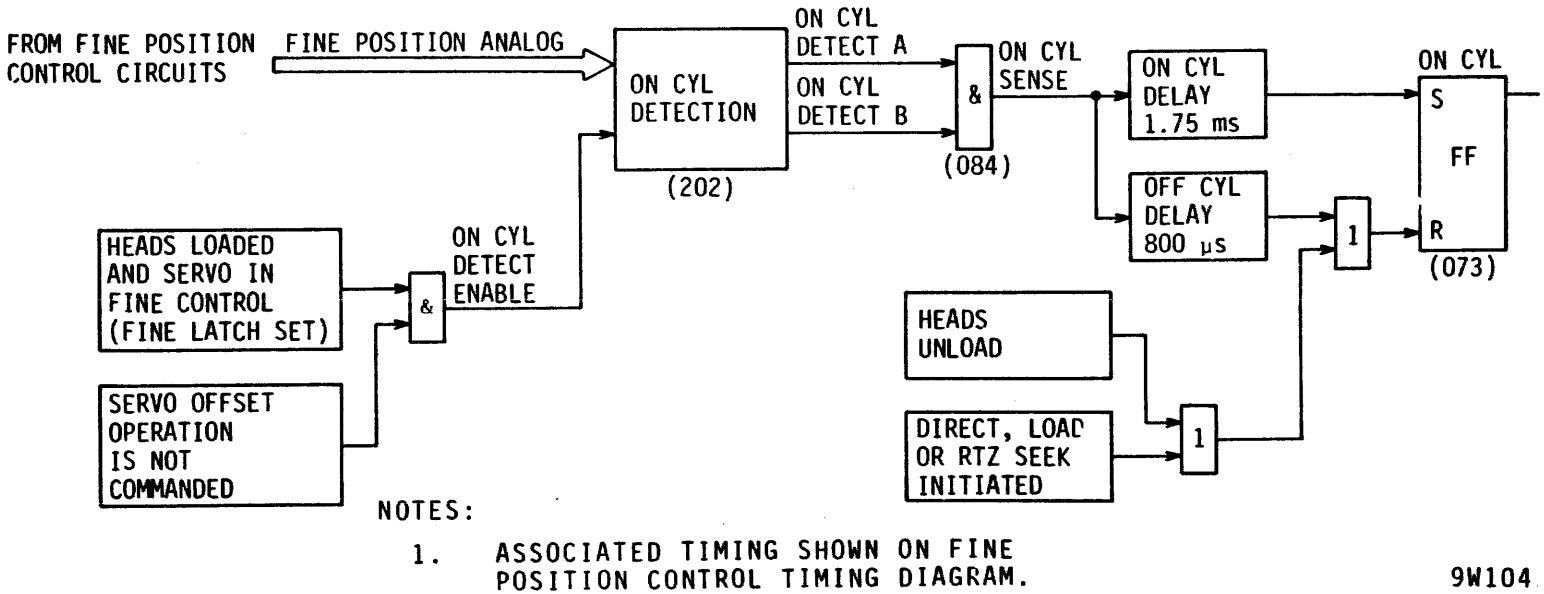


Figure 3-45. On Cylinder Detection Logic

If the heads drift sufficiently to cause a Fine Position Analog signal greater than 0.4 V for more than 800 µs, the Off Cylinder Delay times out causing the On Cylinder FF to clear. This causes a seek error to be generated (refer to discussion on Seek End and Seek Error Detection).

It is possible for the controller to command the drive to move the heads slightly off the track centerline via a write to the error recovery register if it is necessary for data recovery. This is done via an Error Recovery Command (Tag 3 and either Bus Bit 2 or Bus Bit 3 active.

If Bus Bit 2 (Servo Offset Plus) is active, the heads move about 250 microinches towards the spindle. If Bus Bit 3 (Servo Offset minus) is active, the heads move about 250 microinches away from the spindle.

In both cases, the bias signal is summed with the normal position signal at the input to the fine position amplifier (refer to figure 3-43). This causes the carriage to move until the Track Servo signal, which is of a polarity to move the heads back to the centerline, equals and cancels the bias signal.

LOAD SEEK POSITION CONTROL

General

During a load seek, the heads move from the fully retracted position and position out over the disk pack at cylinder 000.

The load seek must be successfully completed before the drive can respond to a read, write or seek command from the controller. When the sequence is completed, the On Cylinder line goes true and the READY indicator on the drive's control panel lights.

The seek is initiated at the same time as the power on sequence by pressing the START switch. However, the actual positioning does not begin until after the power on sequence is complete (disk pack is up to speed). The positioning is divided into coarse and fine modes which are explained in the following. The power on sequence is described in the Power System Discussion.

Figure 3-46 is a flow chart of the entire load sequence (except for power on).

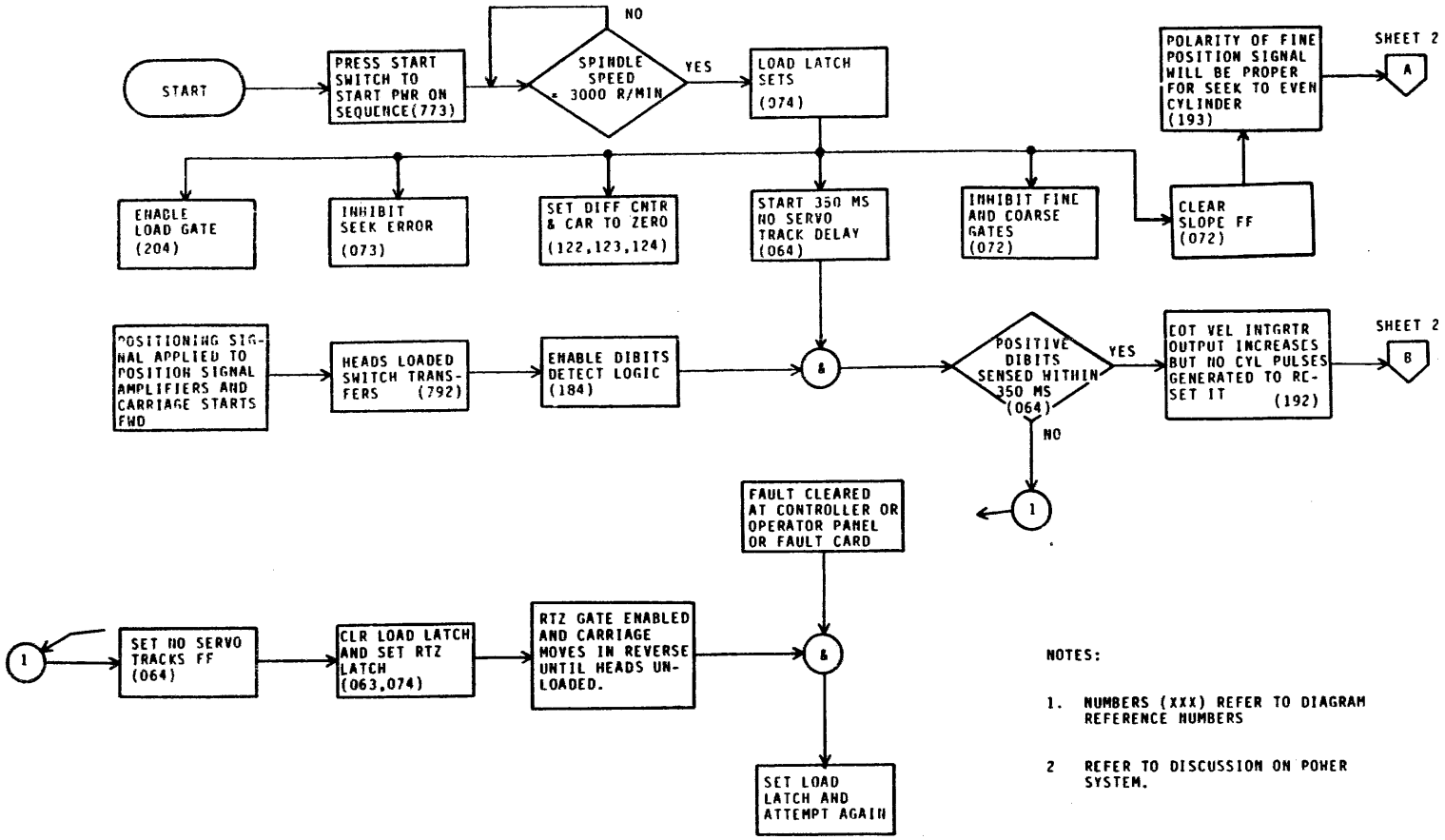


Figure 3-46. Load Sequence Flow Chart (Sheet 1 of 2)

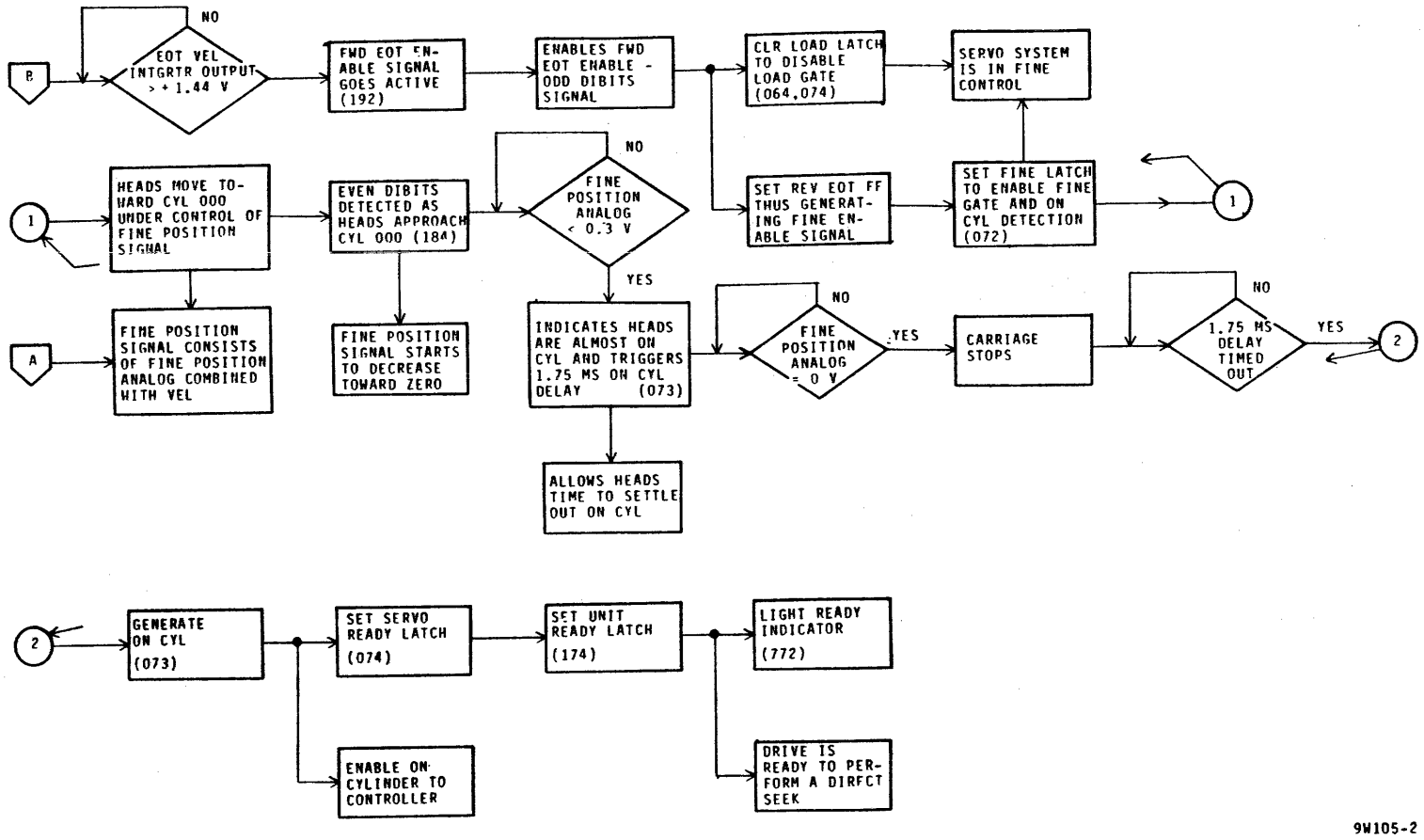


Figure 3-46. Load Sequence Flow Chart (Sheet 2)

Load Seek Coarse Control

The servo system is under coarse control from the time the load is initiated until the reverse end-of-travel zone (refer to discussion on Servo Disk Information) is detected. The circuits involved are shown on figure 3-47 and the timing is on figure 3-48.

The load seek coarse control sequence begins when the power on sequence has been completed and the disk has reached 3000 revolutions per minute. At this time, the Load latch sets and enables the Load gate. The Load gate combines a bias signal with the Velocity signal and applies the resultant signal to the position signal amplifiers. This causes the carriage to move forward at about seven inches per second.

As the heads move forward from the retracted position, the heads loaded switch transfers to the heads loaded position thus enabling the dibits sense logic (refer to discussion on Dibits Sensing). The drive now starts searching for the positive-odd dibits indicating the reverse end of travel area.

Because the heads are moving in a forward direction and the polarity of the Velocity signal is such as to cause the Forward EOT Enable signal to go active (refer to discussion on End-of-Travel Detection), when positive-odd dibits are detected, the Forward EOT°Odd Dibits signal also goes active. This causes the Load latch to clear thus disabling the Load gate. It also sets the Reverse EOT FF which in turn causes the Fine latch to set thus enabling the Fine gate. The carriage is now controlled by the fine position control circuits (refer to figure 3-48).

If for any reason the dibits signals are not detected within 350 ms after the Load latch is set, the RTZ latch sets and the heads unload to the fully retracted position. This also causes the Fault latch to set and FAULT indicator to light.

Pressing the FAULT switch (extinguishing the indicator) clears the fault latch and initiates another load seek. However, the heads will unload again thus lighting the FAULT indicator and setting the Fault latch if dibits are not detected within 350 ms.

Load Seek Fine Control

The fine positioning signal used during load seek fine control is the same as is used during direct seeks and the component of this signal that varies with distance to the destination is also derived from the Track Servo signal.

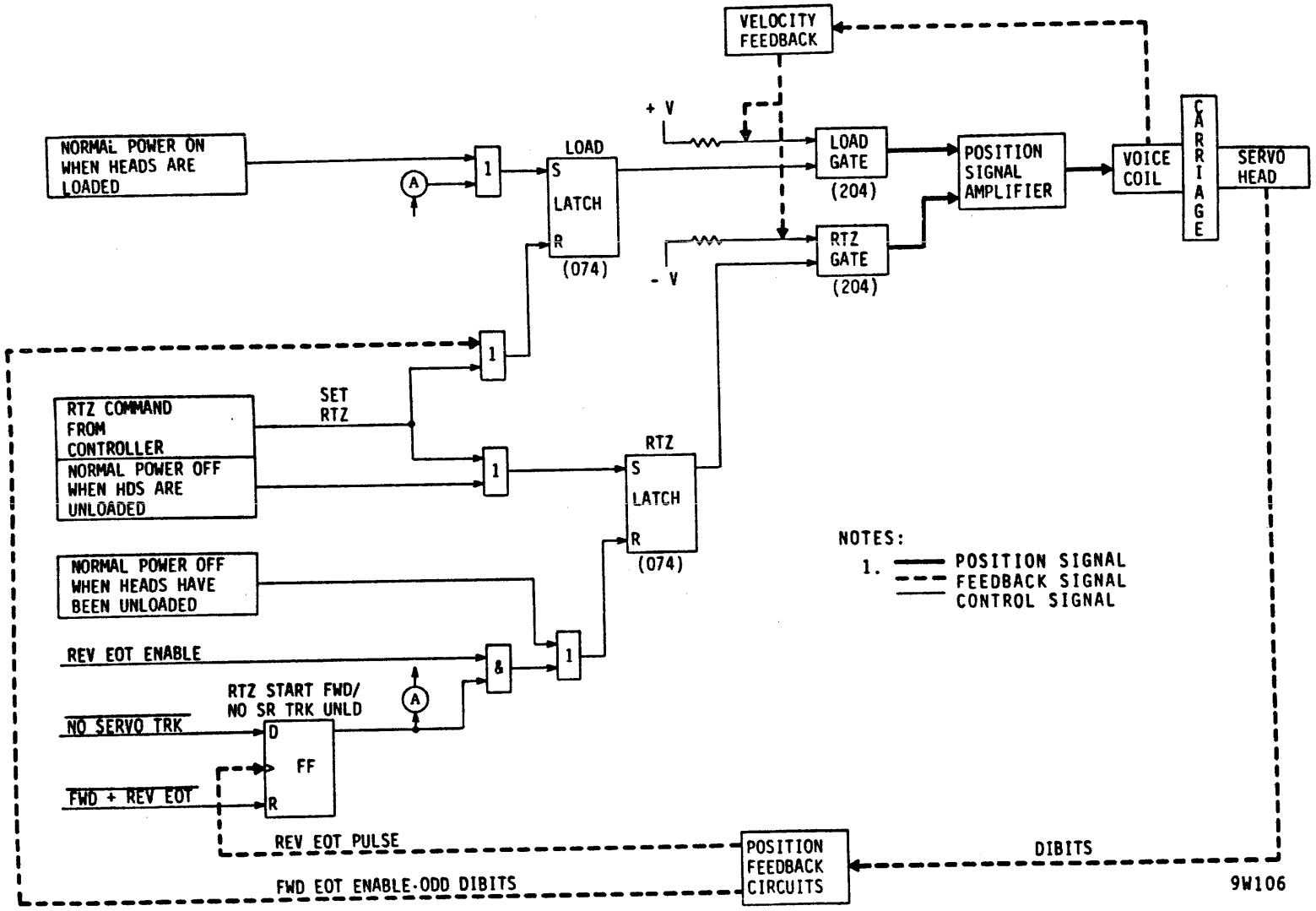


Figure 3-47. Load Seek Circuits

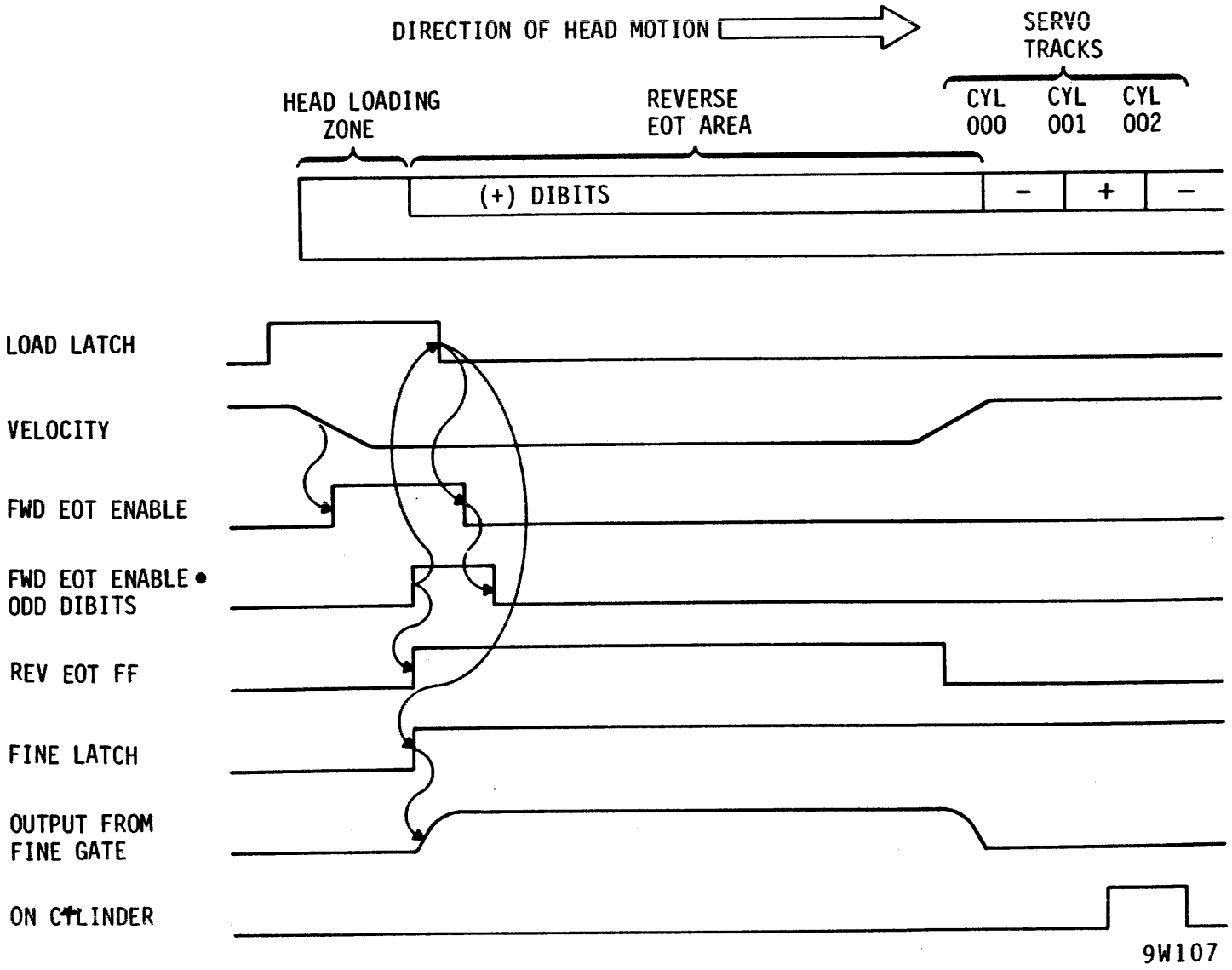


Figure 3-48. Load Seek Timing

Therefore, because the heads are over the reverse end of traveland all positive-odd dibits are being detected, the Track Servo signal is at its maximum negative value and the Fine Position Analog signal (derived from it) is at its maximum positive value. This value is such that a constant forward motion is obtained at the proper speed.

When the heads approach cylinder 000, negative-even dibits are detected. This causes the Track servo signal, and therefore the Fine Position Analog signal to decrease towards zero. The carriage now decelerates and servos onto the on cylinder position. On Cylinder detection and track following is the same as discussed for direct seeks.

RETURN TO ZERO SEEK POSITION CONTROL

The return to zero seek (RTZS) function is an alternate means for the controller to command the drive to seek to cylinder 000 without issuing a direct seek command. This might be necessary in cases where a seek error has occurred.

The controller initiates a return to zero seek via a Tag 3 accompanied by Bus Bit 6 (RTZ). When the drive receives this command, the RTZ latch sets and enables the RTZ gate (refer to figure 3-50). The RTZ gate, like the Load gate, combines a bias signal with the Velocity signal and applies the result to the position signal amplifiers. However, in this case the resultant signal causes the carriage to move in reverse at about seven inches per second.

When the carriage moves past cylinder 000, it enters the reverse end of travel area and no more cylinder pulses are generated. The loss of cylinder pulses allows the EOT Velocity Integrator output (which is normally reset to zero by cylinder pulses) to exceed -1.4 V.. This causes the Reverse EOT Enable signal to go true and set the Reverse EOT Enable FF (Refer to discussion on End of Travel Detection). Setting the Reverse EOT FF causes the Velocity Integrator to reset but the carriage continues moving in reverse and the integrator output starts to rise again.

After an additional reverse motion of about two tracks, the Velocity Integrator output again exceeds -1.4 V. This time the Reverse EOT Enabvle signal enables the Set Load signal which sets the Load latch and clears the RTZ latch.

Setting the Load latch causes the carriage to reverse direction and start back towards cylinder 000. During the remainder of the operation, the drive seeks to cylinder 000 as during a load sequence (refer to discussion on Load Seek Position Control).

Figure 3-49 shows the timing for and figure 3-50 is a flow chart of the entire return to zero seek function.

UNLOAD HEADS POSITION CONTROL

The heads are normally unloaded at the start of the power off sequence (refer to discussion on Power System). This is necessary to make certain the heads are not over the disk when it slows down as this would cause head crash. The heads are also unloaded during certain error conditions (refer to discussions on Emergency Retract and Seek End and Seek Error Detection). The following describes the heads unload sequence occurring during a normal power off.

The sequence is initiated when the START switch is pressed and the power supply circuits generate signals that set the RTZ latch (refer to discussion on Power System). Setting the RTZ latch enables the RTZ gate and the carriage starts retracting at seven inches per second. The action is similar to an RTZ except that the EOT detection circuit is disabled so that the Reverse EOT Enable signal never goers active. Therefore, the RTZ latch remains set and motion continues until the heads unload.

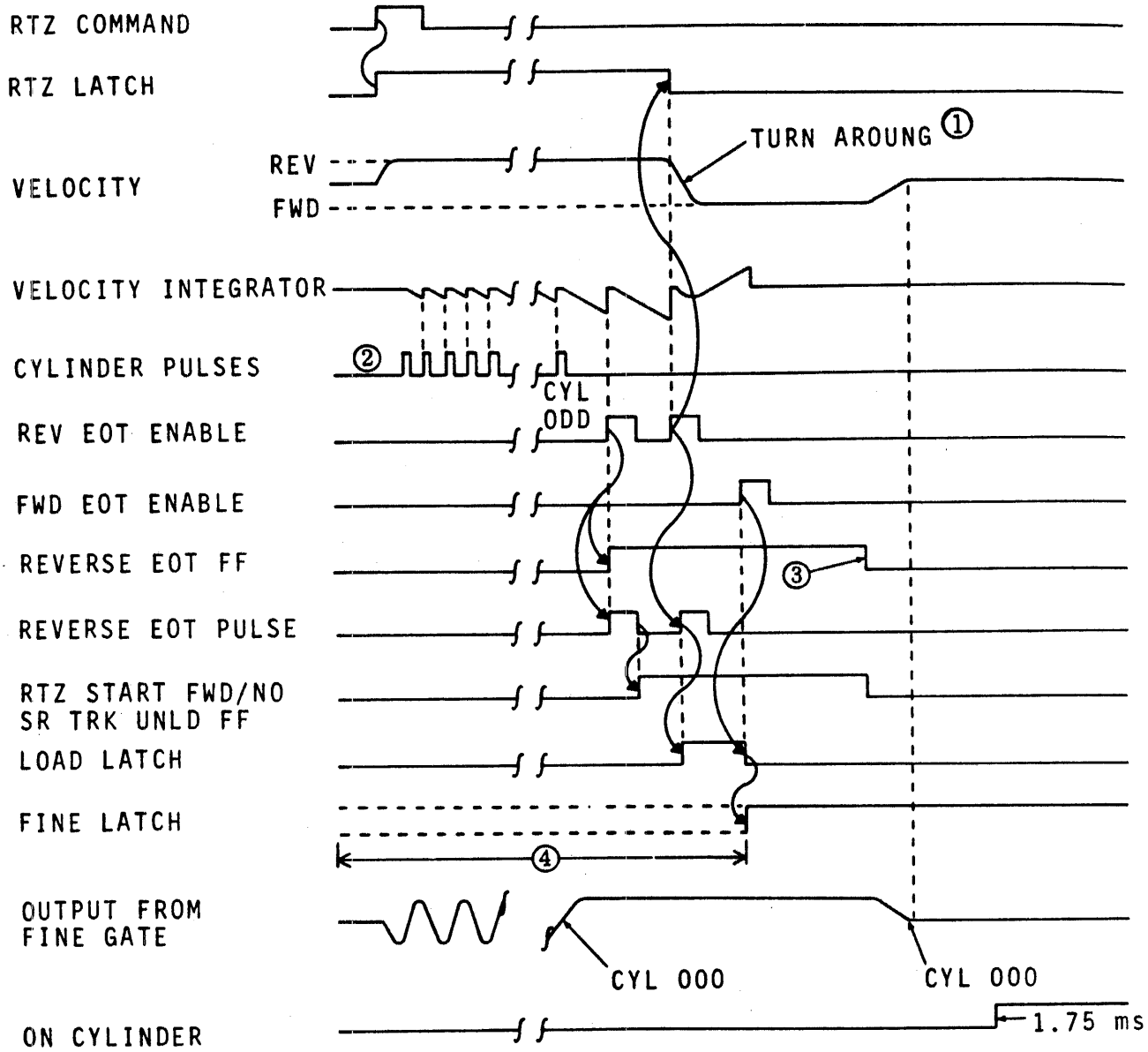
When the heads loaded switch transfers, indicating the heads are unloaded, the RTZ latch is cleared. This disables the current to the voice coil and the carriage stops driving in reverse. However, the power off sequence continues and this is described in the discussions on the Power System.

SEEK END AND ERROR DETECTION

General

Successful completion is indicated when the drives On Cylinder signal is active and the Seek Error latch is not set. An unsuccessful seek is indicated whenever the Seek Error latch is set (either with or without On Cylinder). This occurs if the drive cannot complete the seek or if an error occurs during the seek operation. If the seek error latch is set, the drive cannot perform another seek until the latch is cleared. This is done via an RTZ command (Tag 3, Bus Bit 6).

The controller determines whether the seek was successful or unsuccessful by monitoring the On Cylinder and Seek Error lines. Whn On Cylinder is true it indicates heads are positioned over a cylinder and when Seek Error is true it indicates a seek error has occurred.



NOTES:

1. CLEARING RTZ AND SETTING LOAD LATCH CAUSES CARRIAGE TO REVERSE DIRECTION AND MOVE FWD.
2. CYLINDER PULSES RESET VELOCITY INTEGRATOR.
3. REV EOT FF CLEARED WHEN NEGATIVE-EVEN DIBITS ARE DETECTED AS HEADS APPROACH 000.
4. FINE LATCH IS JAMMED (BOTH INPUTS HIGH) THUS DISABLING BOTH COARSE AND FINE GATES AS LONG AS EITHER LOAD OR RTZ LATCH IS SET

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Figure 3-49. Return to Zero Seek Timing

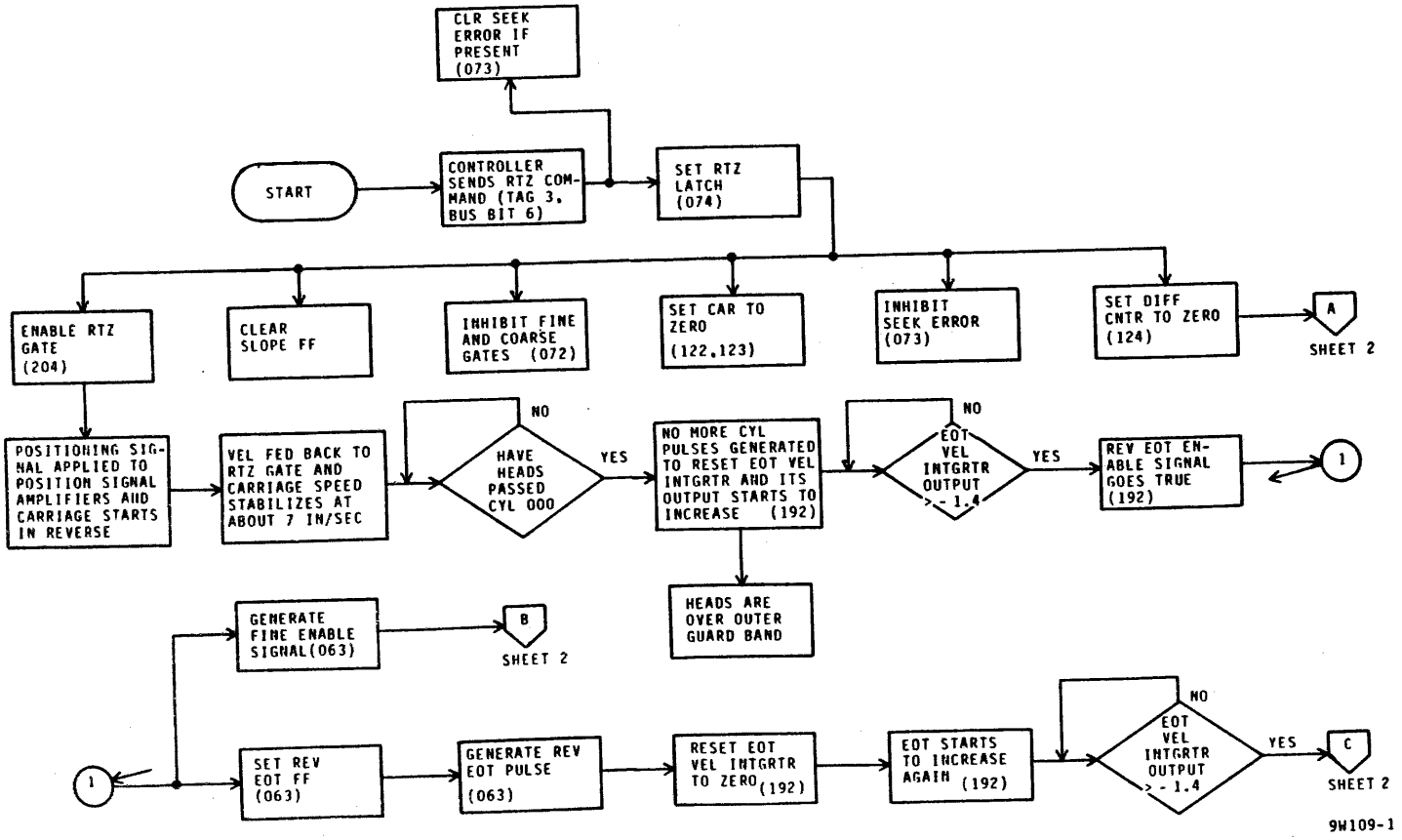


Figure 3-50. Return to Zero Seek Flow Chart (Sheet 1 of 2)

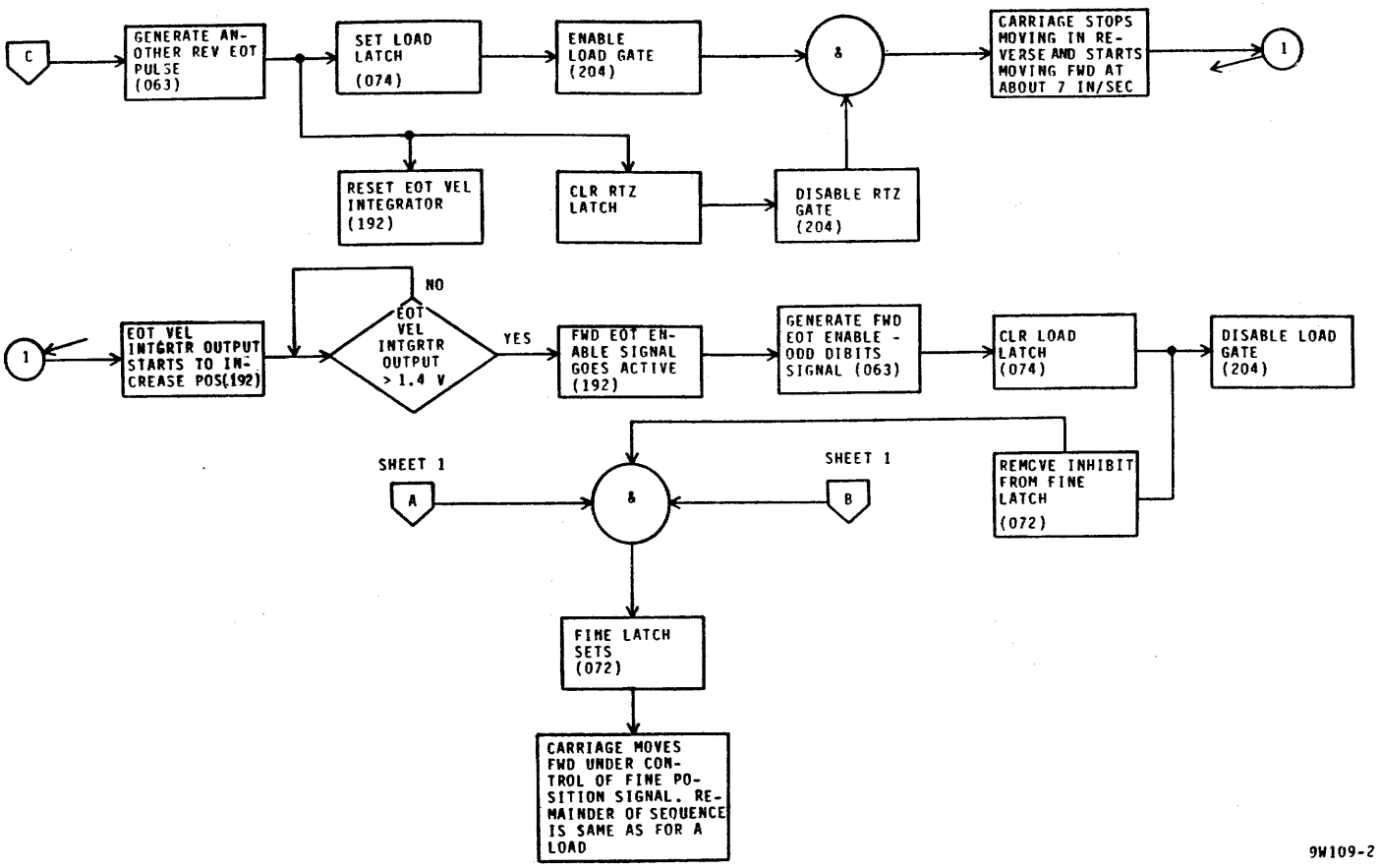


Figure 3-50. Return to Zero Seek Flow Chart (Sheet 2)

The conditions interpreted by the drive as seek error are described in the following paragraphs. The basic logic is shown on figure 3-51.

Timeout Error

If the drive does not generate On Cylinder within 500 ms of the start of the seek, the Seek Error latch sets.

Setting the Seek Error latch causes the Difference counter to be reset to zero and the Slope FF to be cleared. This causes the drive to seek to the nearest even numbered cylinder and generate On Cylinder.

Maximum Address Fault

If the controller commands the drive to seek to a cylinder address greater than 822 the Seek Error latch is set and the drive will not perform the seek.

End-of-Travel Errors

General

Whenever a direct seek is being performed and the heads are positioned outside of the normal data area, an end of travel condition exists and the Seek Error latch sets.

It is possible for the heads to be positioned over either the forward or reverse end-of-travel area and both of these sequences are described in the following (also refer to discussion on End-of-Travel Detection).

Forward End-of-Travel

When the heads move past cylinder 822 they enter the forward end-of-travel area (inner guard band).

Because cylinder pulses are not generated as the heads move over this area, the EOT Velocity Integrator output is able to exceed +1.35 V (refer to discussion on End of Travel Detection). This causes the Forward EOT Enable signal to go active and set the Forward EOT FF.

This causes the following:

- Seek Error latch sets thus causing a Seek End to the controller.

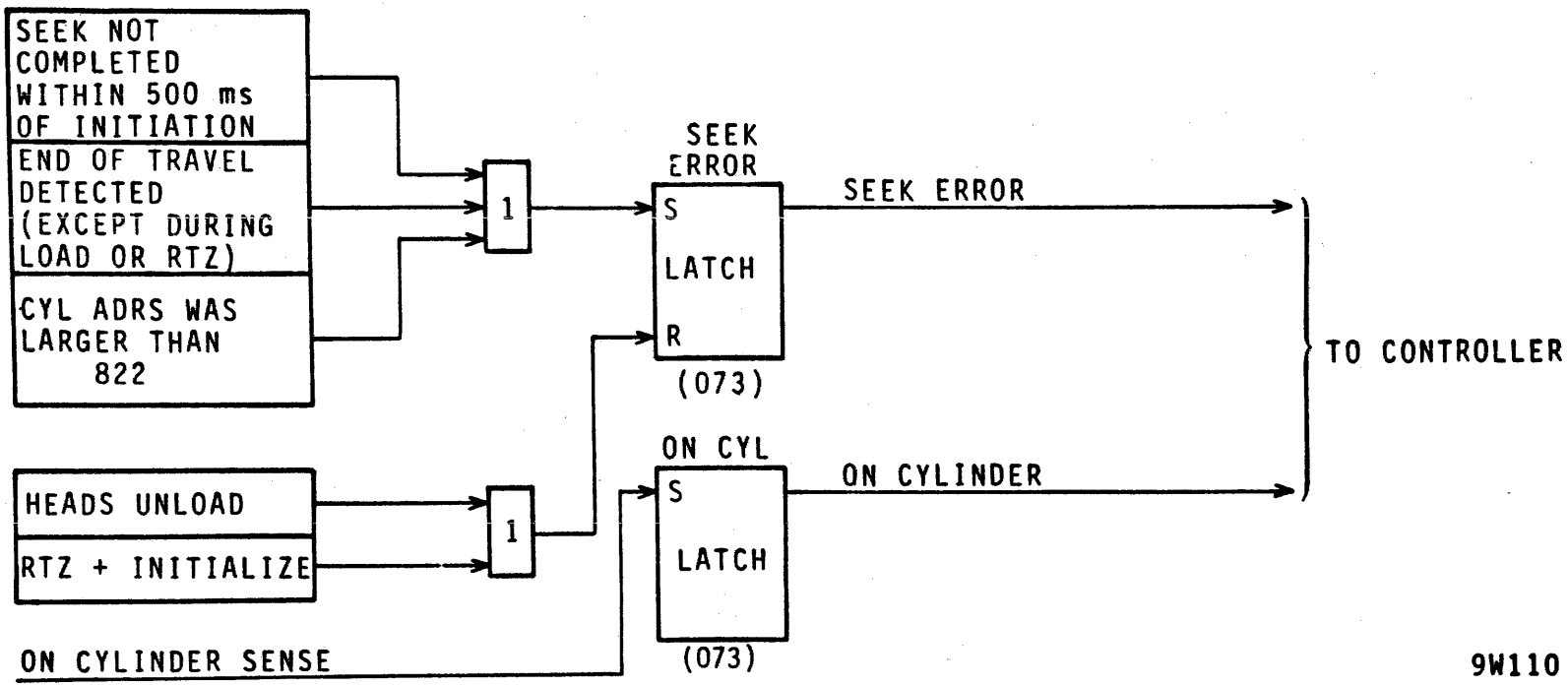


Figure 3-51. Seek End and Seek Error Detection Logic

- Seek FF (set at start of seek) clears.
- Difference counter set to 000 (T=0).
- Fine Enable signal goes active.
- Slope FF is cleared to indicate a seek to an even numbered cylinder.

When the Fine Enable signal is active and the Difference counter equals zero the Fine latch is enabled thus enabling the Fine gate.

Because the heads are over the inner guard band and all negative-even dibits are being detected, the Track Servo signal is at its maximum positive value. This results in a Fine Position Analog signal that is at its maximum negative value and the carriage moves in reverse towards cylinder 822.

When cylinder 822 is approached, positive-odd dibits are detected, the Track Servo and Fine Position Analog signals decrease, and the carriage decelerates until it is on cylinder at physical cylinder 822. The heads remain at this location until the drive receives an RTZ command.

Reverse End-of-Travel

A Reverse End-of-Travel condition indicates the heads have moved in reverse past cylinder 000 and into the outer guard band.

When this occurs, the Reverse EOT FF sets and initiates a load sequence that returns the heads to cylinder 000. The heads remain at this location until the drive receives an RTZ command which clears the Seek Error latch.

MACHINE CLOCK

General

The machine clock circuits generate the clock signals necessary for drive operation. These circuits are divided into two areas (1) Servo Clock Multiplier and (2) Write Clock Multiplier. These are both explained in the following discussions.

SERVO CLOCK MULTIPLIER

The servo clock multiplier circuits generate clock pulses used by the sector detection, Index detection and the Read PLO circuits. It also generates the 9.67 MHz Servo Clock signal that is sent to the controller.

The main element in the servo clock multiplier circuit is the phase lock loop. This loop consists of a phase and frequency detector, error amplifier, voltage controlled oscillator and a divide by 12 circuit. The function of the loop is to adjust itself until its output is identical in phase and frequency to its input.

The input to the loop consists of the dibit signals from the track servo circuit. The nominal frequency of these signals is 806 kHz; however, their actual frequency is a function of and varies directly with disk pack speed. This means that the output of the loop will also vary with disk pack speed.

The phase and frequency detection circuit makes the comparison between the input dibits and the output of the loop.

The input dibits are applied via two retriggerable multivibrators. One of these multivibrators provides a 750 ns (approximate) output pulse which is then fed through a pulse forming circuit to provide a 25 ns input pulse for the phase and frequency detector. These pulses vary at the dibit frequency. The other multivibrator has a 1.6 microsecond output which is used to enable the feedback pulses from the loop output to the input of the phase and frequency detector. The 1.6 microsecond pulse is longer than the period of the nominal dibit frequency (806 kHz); therefore, the feedback pulses are continuously gated as long as dibits are present.

The outputs from the detector are fixed amplitude pulses which are a function of the time (or phase) difference between the positive going edges of the two inputs (refer to figure 3-52).

These outputs are applied to the error amplifier which integrates them and generates a voltage proportional to the phase difference between them. This voltage is used as a control voltage for the voltage controlled oscillator.

The control voltage causes the VCO frequency to vary in the direction necessary to eliminate the phase or frequency difference between the input and output of the loop. The VCO output is then divided by 12, by the divide by 12 circuit, and fed back to the loop input.

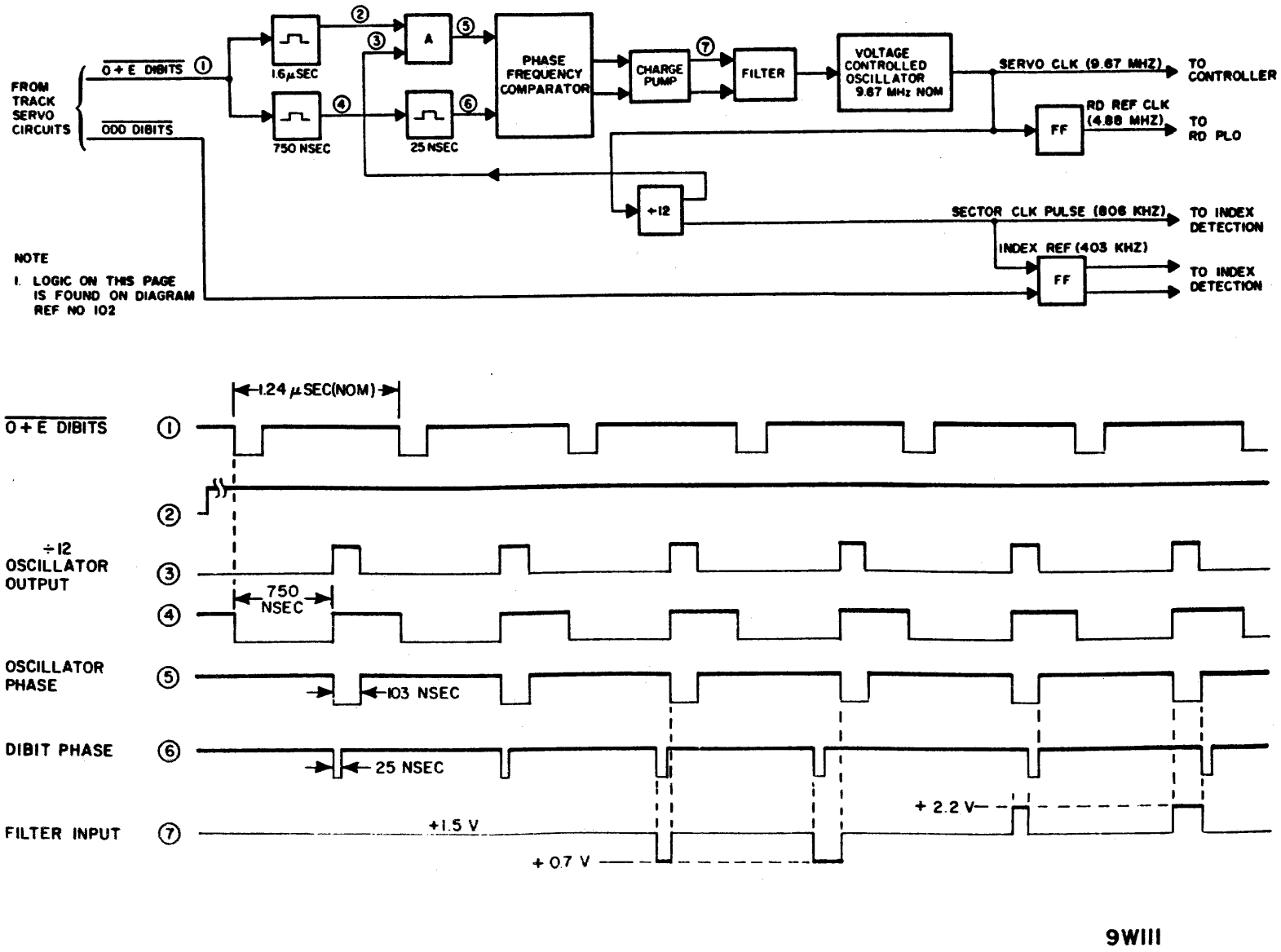


Figure 3-52. Servo Clock Multiplier

When the VCO output is 9.67 MHz, the feedback provided by the divide by 12 circuit will be 806 kHz and the loop will be synchronized.

Both the 9.67 MHz and 806 kHz signals are divided by two thus producing 4.84 MHz and 403 kHz signals. All four of these frequencies are used by the drive as shown on figure 3-52.

WRITE CLOCK FREQUENCY MULTIPLIER

The write clock frequency multiplier circuit (refer to figure 3-53) generates the 19.34 MHz and 9.67 MHz signals used during write operations.

This circuit consists mainly of a phase lock loop and operates essentially the same as the servo clock multiplier. However, the input to the write clock multiplier is the 9.67 MHz Write Clock signals from the controller. The phase lock loop synchronizes to these signals and provides the 19.34 MHz and 9.67 MHz outputs. These outputs are used by the NRZ to MFM converter and Write Compensation circuits during write operations.

INDEX DETECTION

Each track on the servo disk contains a pattern of missing dibits referred to as the Index pattern. When the drives Index Detection circuits (refer to figure 3-54) detect this pattern, they generate a 2.5 microsecond Index signal. The Index signal indicates, both to the drive and controller, the logical beginning of a track.

The Odd Or Even Dibits signal provides the data necessary to actually detect the missing dibit pattern. This signal is derived from the dibits detected from the disk and has a nominal frequency of 806 kHz. Because this signal is derived from the dibits, whenever a dibit is missing an Odd or Even Dibits pulse is also missing.

Detection of missing dibits is done by the Missing Dibits one shot. This one shot is triggered by the Odd Or Even Dibits signals and will not time out as long as dibits are present. However, if two or more consecutive dibits are missed the one shot times out. The output of the Missing Dibits one shot provides the data input for the first stage of the Index Shift register.

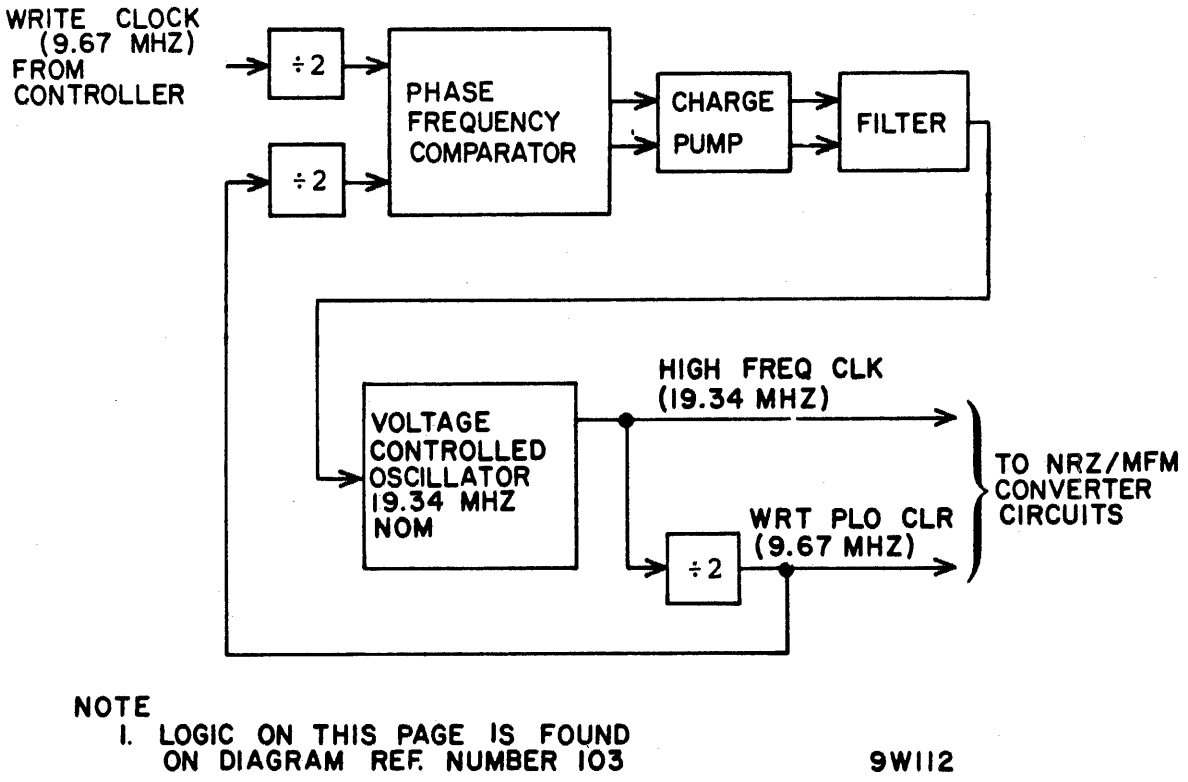


Figure 3-53. Write Clock Multiplier

The Index Shift register loads the output of the missing Dibits one shot into its first stage (and also performs its shift) each time a 403 kHz Index Reference Clock pulse occurs. When the one shot is in a triggered state (indicating dibits were present), a one is loaded into the register. However, when the one shot is timed out (indicating two or more dibits were missing) a zero loads into the register.

The contents of the Index shift register are continuously compared to the Index pattern by the Index Decoder and when the shift register contains the pattern indicating Index has occurred, the Index Decoder generates an Index signal. The missing dibit pattern associated with Index and the pattern contained in the shift register when Index has occurred are shown on figure 3-54.

In summary, the Index detection circuit contains three main elements:

- Missing Dibits one shot - Detects the missing dibits in the Index pattern.
- Index Shift register - Accumulates the dibit pattern so that it can be compared with the pattern occurring during Index.
- Index Decoder - Compares the contents of the Index Shift register with the Index pattern and generates an output signal when Index is detected.

These elements work in conjunction with the two input signals (Odd or Even Dibits and 403 kHz Index Reference Clock) to produce the Index signal. The Index signal is sent to the controller and is also used to reset the drives sector detection circuitry.

SECTOR DETECTION

The sector detection circuits (refer to figure 3-55) generate signals which are used by the system to determine the angular position of the heads with respect to Index. These signals are called Sector pulses and either 30 or 32 of them are generated during each revolution of the disk pack. The Sector pulses logically divide the disk into areas called sectors.

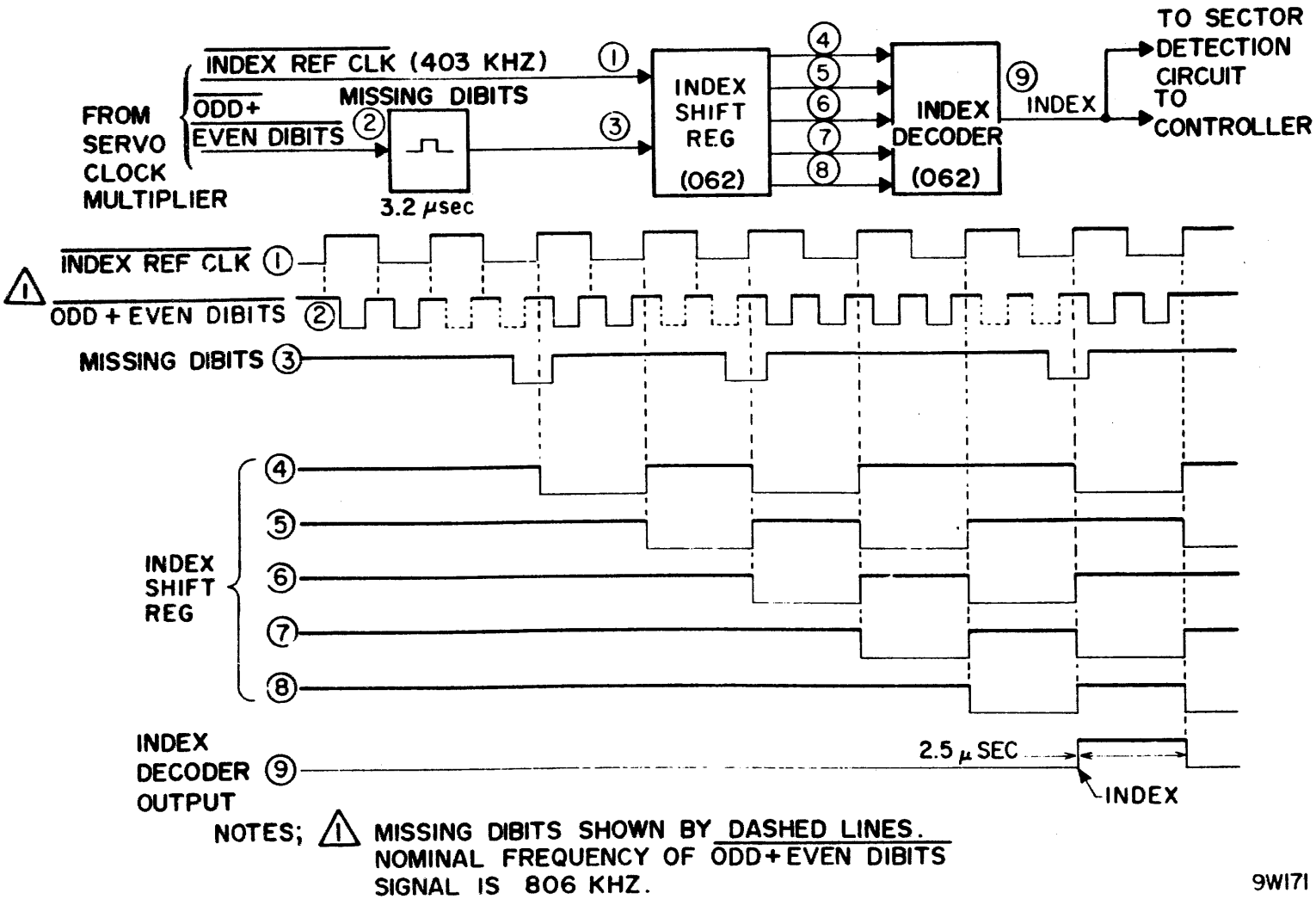
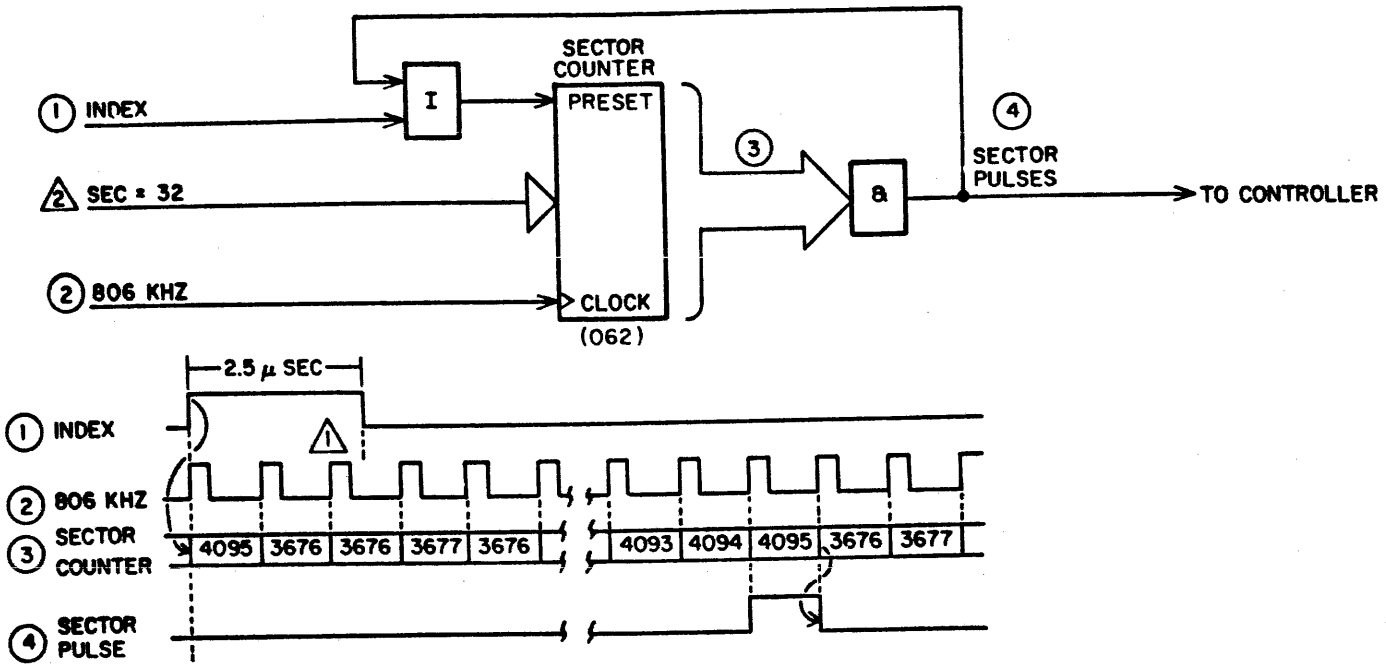


Figure 3-54. Index Detection - Logic and Timing



NOTE:

1. THIS PULSE DOES NOT INCREMENT COUNTER BECAUSE INDEX IS STILL ACTIVE: THEREFORE, SECTOR 000 ALWAYS CONTAINS ONE MORE 806 KHZ PULSE THAN ANY OTHER SECTOR.

2. WHEN SECTOR 30 OR 32 LINE FROM CONTROLLER IS HIGH, COUNTER IS PRESET TO 32 SECTORS.

9W113

Figure 3-55. Sector Detection - Logic and Timing

The controller governs whether there will be 30 or 32 sectors by use of the Sector 30 or 32 line. If this line is high the drive presets the Sector Counter to produce 32 sector pulses. If the line is low, 30 sector pulses are produced. The Sector pulses are generated by the Sector counter, which causes a pulse to be generated each time it indicates its maximum value of 4095.

The Sector counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the servo track dibit signals (refer to discussion on track servo circuit) and exactly 13 440 clock pulses occur during each revolution of the disk pack.

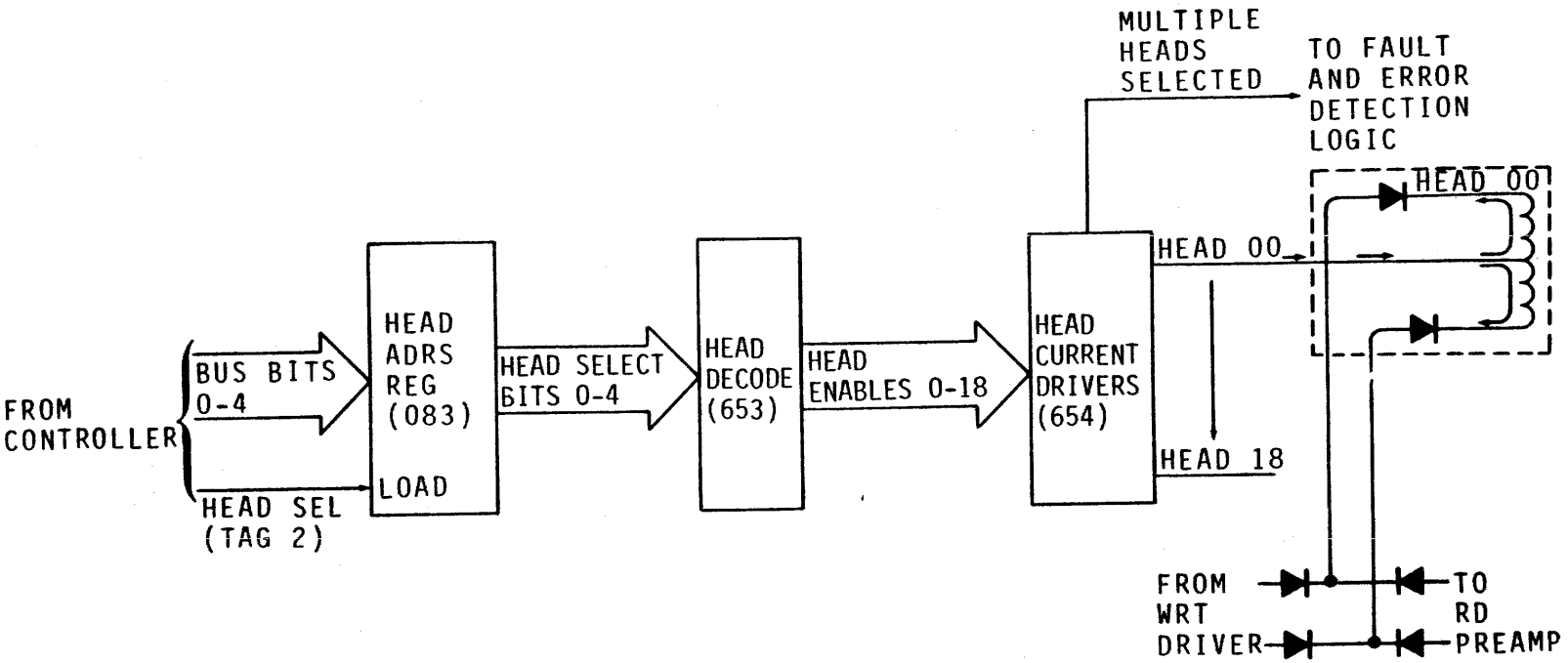
The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) either 30 or 32 times per revolution. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 32 sectors, the counter would have to count 420 clock pulses in each sector (13 440 divided by 32) and the counter would be preset to 3676. In this case the counter starts at 3676 and increments each clock time until it reaches the maximum count of 4095. Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (420) presets the counter back to 3676 (thus disabling the Sector pulse) and the counter begins the next sector. The 3676 is obtained by subtracting 420 from 4096, which is the total number of clock pulses the counter is capable of counting (0 through 4095 = 4096).

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Head selection starts when the controller sends the drive a Head Select tag (2) and a head address. The head address is sent on Bus Bits 0 through 4.

The Head Select tag gates the address into the Head Address register. This address is then decoded to a Head Enable signal (0 through 18 depending on bus 0 Bits 0 through 4). This signal then enables the head current driver associated with the addressed head and allows the head to conduct as shown on figure 3-56.

If more than one head is selected, a fault is indicated (refer to discussion on Fault and Error Conditions).



NOTE:

1. NUMBERS (XXX) REFER TO DIAGRAM REF. NO.

Figure 3-56. Head Select Circuits

READ/WRITE FUNCTIONS

General

When the drive is on cylinder and has a head selected, it is ready to perpform a read or write operation. The controller initiates a read or write operation by sending the drive a Control tag (3) and the proper bus bits (refer to discussion on Interface function).

During a read operation, the drive recovers data from the disk and transfers it to the controller. During a write operation, the drive receives data from the controller and records it on the disk.

Figure 3-57 is a block diagram of the read/write circuits. The remainder of this discussion describes the read/write circuits and is divided into the following areas:

- Basic Read/Write Principles - Explains the basic principles of recording data on and recovering data from a magnetic disk.
- Read Circuits - Describes the circuits used by the drive to recover data from the disk.
- Write Circuits - Describes the circuits used by the drive to record data on the disk.

BASIC READ/WRITE PRINCIPLES

General

Information is recorded on and read from the disk by the read/write heads. The following discusses the physical principles involved and techniques used in this process.

Writing Data on Disk

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (figure 3-58). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a North pole and a South pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

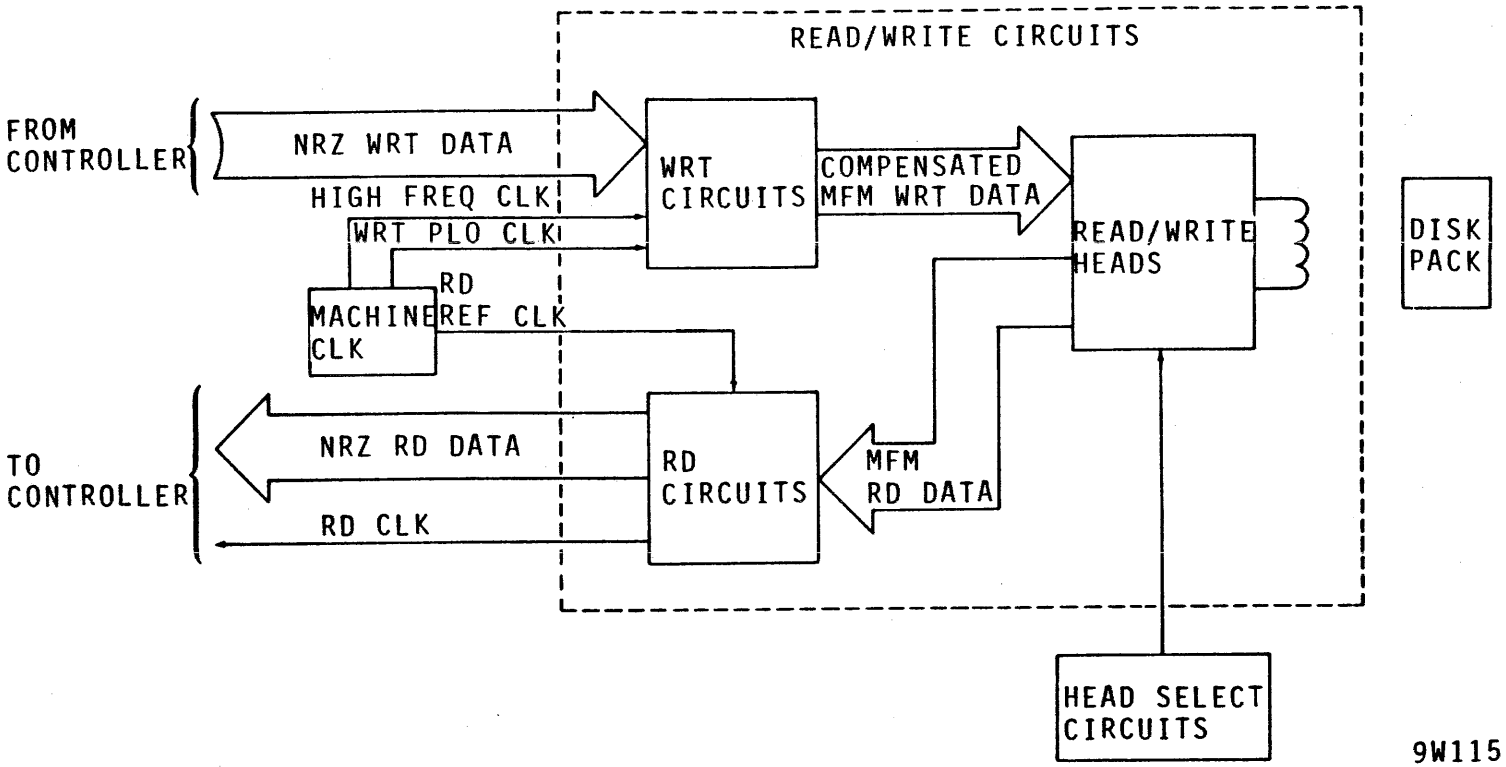
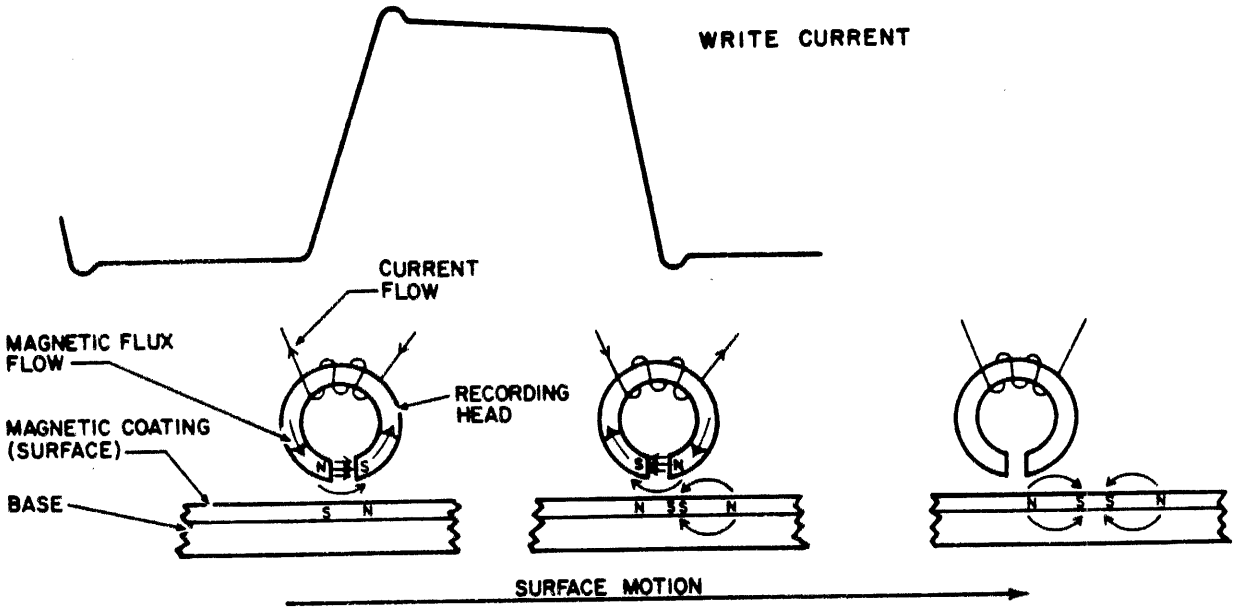


Figure 3-57. Read/Write Circuits Block Diagram



NOTE: RELATIVE HEAD TO SURFACE MOTION, RECORDING (WRITE OPERATION) 7S17A

Figure 3-58. Writing Data

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field across the gap. The flux change defines a data bit.

Erasing old data is accomplished by writing over any data which may already bo on the disk. The write current is zoned in eight current zones to ensure proper saturation level for best head resolution. The write current is maximum on the outer tracks and progressively decreased for inner tracks.

Reading Data From Disk

As the disk passes beneath the read/write head, the stored flux intersects the gap (figure 3-59). Gap motion through the flux induces a voltage in the head windings. This voltage is analyzed by the read circuit to define the data recorded on the disk. Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

Peak Shift

Peak shift is an effect that degrades read accuracy by distorting the waveform. This condition exists because no electromechanical device can be perfect.

Ideally, the flux reversal command by the write toggle would be instantaneous as shown in the Ideal Recording portion of figure 3-60. Current would immediately switch from one polarity to the other. As a result, the distance required to complete the magnetic flux reversal on the disk would be so narrow as to be insignificant; the readback pulse would then also be extremely narrow. To carry the principle one step further, the heads would be an infinitesimal distance from the disk surface. Therefore, the head gap itself could be made very small for two reasons:

- The magnetic field strength increases as the head moves closer to the disk.
- The head gap must be wide enough to intersect sufficient lines of force from the magnetic flux field to generate a signal. The weaker the signal, the wider the gap must be. With the substantial flux amplitude gained by having the head very close to the disk surface, a very small head gap can generate a reliable readback voltage.

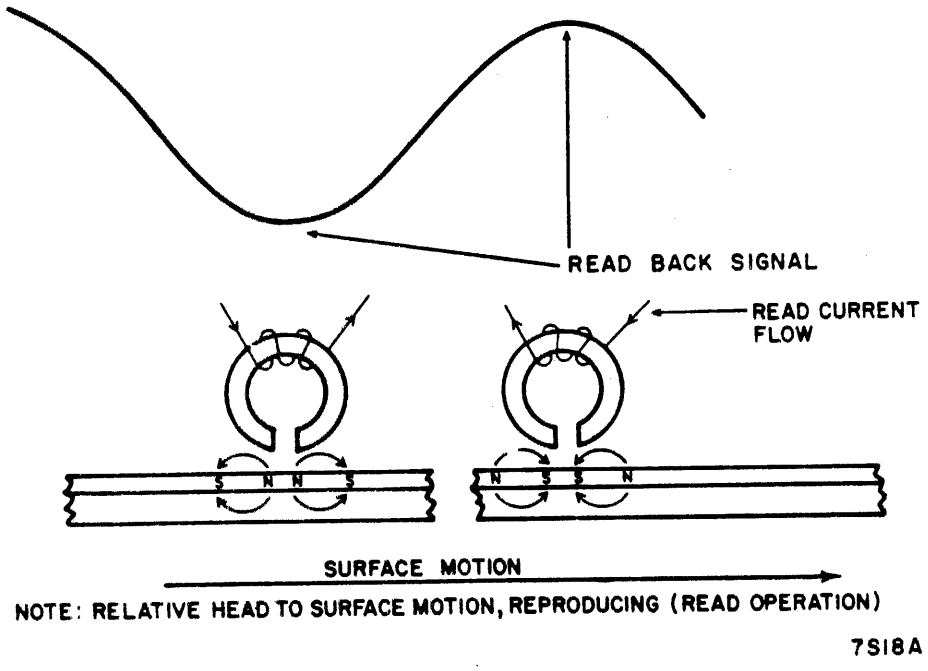


Figure 3-59. Reading Data

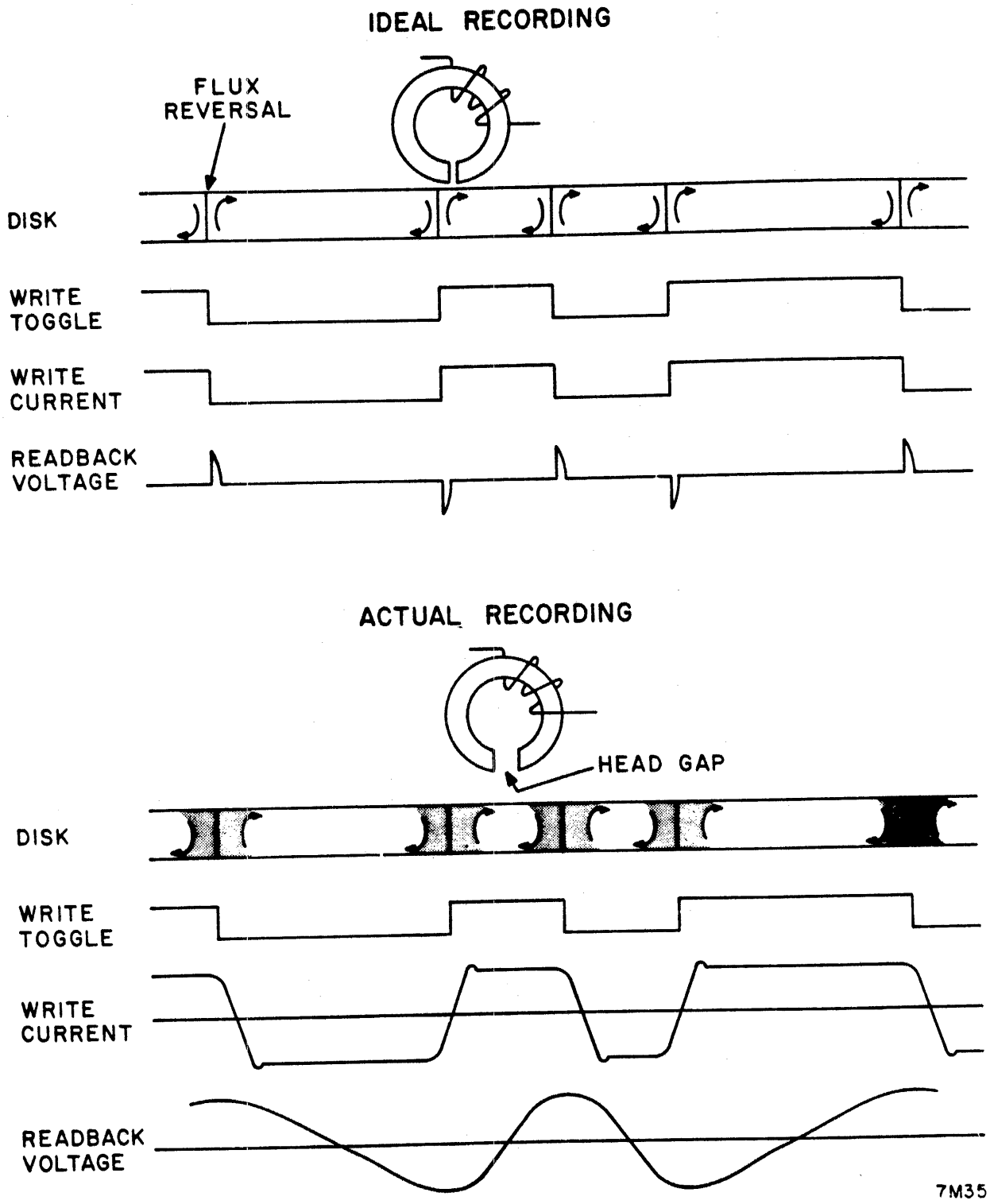


Figure 3-60. Write Irregularity-Typical Waveforms and Timing

However, it takes time for the current to reverse, and the flux change is not instantaneous. Furthermore, heads must fly a finite distance from the disk. The greater the distance between the head and the oxide, the wider the head gap must be. The resulting readback voltage is more or less sinusoidal with peaks less easily defined in time or amplitude.

With modern high frequency recording techniques, adjacent clock/data pulses are close enough to interact with each other. This is shown in figure 3-61. Peak shift is the result of the interaction of the pulses. Because two pulses tend to have a portion of their individual signals superimpose themselves on each other, the actual readback voltage is the algebraic summation of the pulses.

When all "1's" or all "0's" are being recorded, the data frequency is constant: pulses are placed apart by one cell (103 ns). As a result, the pulse spacing causes the overlap errors to be equal and opposite. The negative-going and positive-going errors cancel each other. This is the "zero peak shift" condition of the "...111..." pattern in figure 3-61.

Peak shift occurs when there is a change in frequency. A "011" pattern represents a frequency increase since there is a delay of about 1.5 cell between the "01" and only 1.0 cell between the "11". As a result, the squeezing of the cells causes the mathematical average (the actual readback voltage) to shift the apparent peak to the left. This is early peak shift.

On the other hand, a "10" pattern represents a frequency decrease since a pulse is not written at all in the second cell. In addition, a "001" pattern is also a frequency decrease since there is a 1.0 cell interval between the first two bits and 1.5 cell between the last two bits.

The examples listed above examined only two or three bits without regard to the preceding or subsequent data pattern. The actual combinations are somewhat more complex. The drive logic examines and defines the following patterns:

Pattern	Frequency Change
.011	Increasing
1000	Increasing
..10	Decreasing
.001	Decreasing

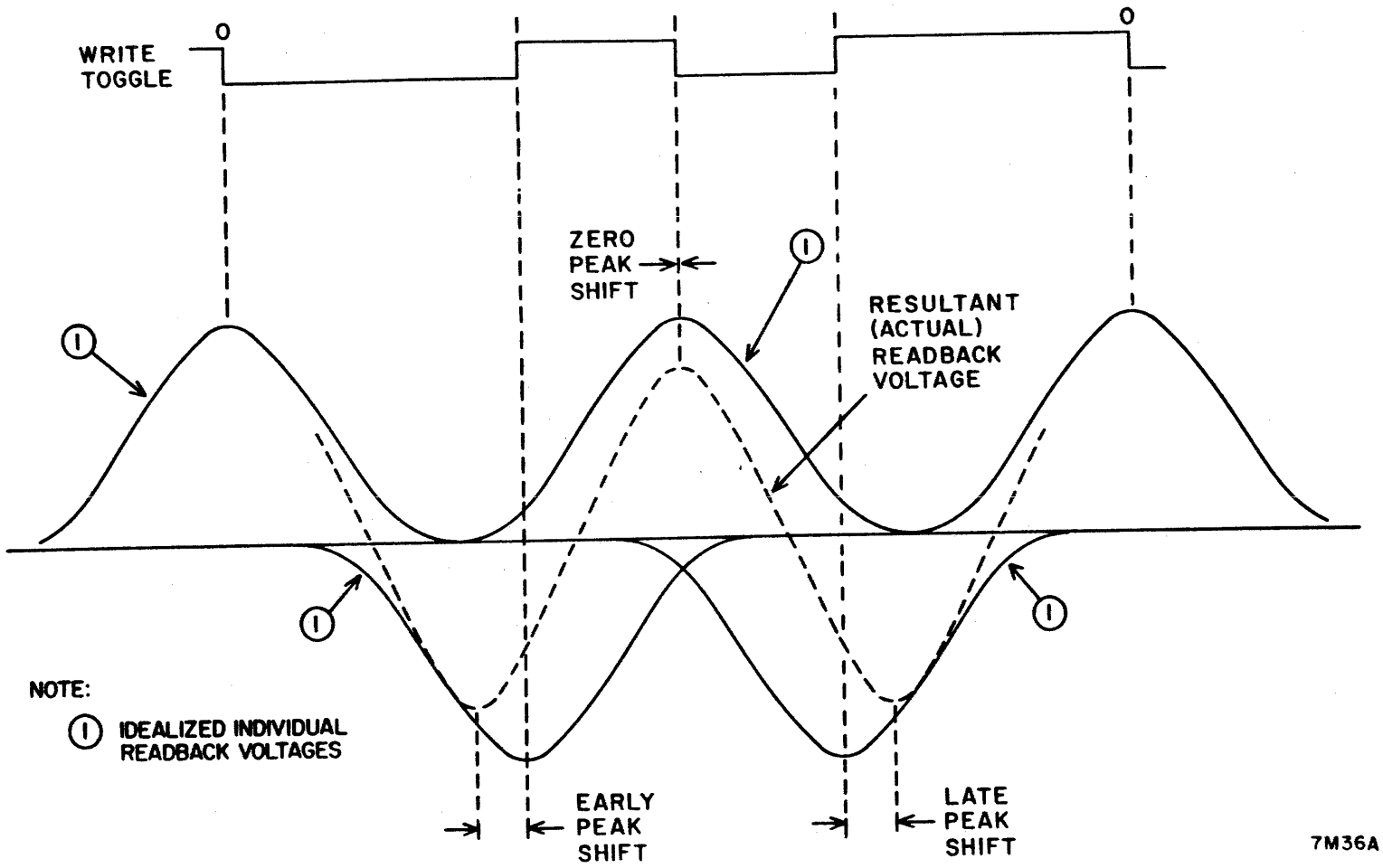
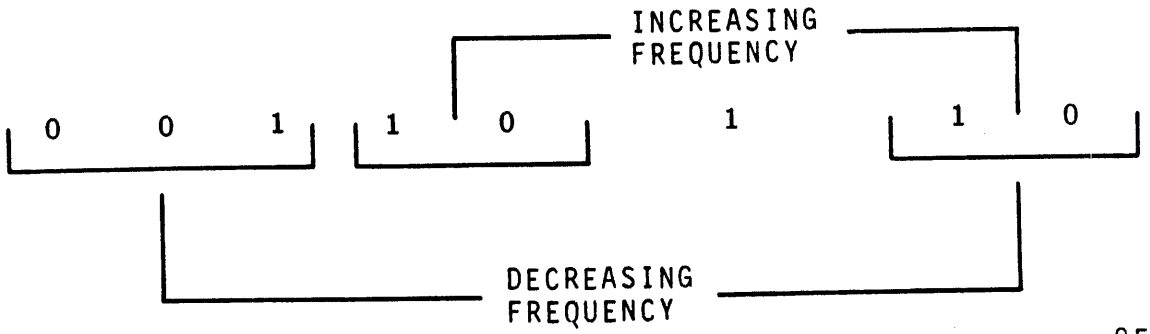


Figure 3-61. Peak Shift Timing



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Any data pattern will have considerable overlapping of the data pattern frequency changes. Consider the overlap of these basic eight bits:

Any of these peak shift conditions can cause errors during subsequent read operations. The device compensates for these known errors by intentionally writing a pulse earlier or later than nominal. This function is accomplished by the write compensation circuit.

Principles of MFM Recording

In order to define the binary dibits stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation technique.

The length of time required to define one bit of information is the cell. Each cell is nominally 103 ns in width. The data transfer rate is, therefore, nominally 9.677 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (figure 3-62). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rules for MFM recording may be summarized as follows:

- There is a flux transition for each "1" bit at the time of the "1".
- There is a flux transition between each pair of "0" bits.
- There is no flux transition between the bits of a "10" or "01" combination.

The advantages and disadvantages of MFM recording are as follows:

- Fewer flux reversals are needed to represent a given binary number because there are no flux reversals at the cell boundaries, achieving higher recording densities of data without increasing the number of flux reversals per inch.
- Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.
- Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media to be accomplished.

READ CIRCUITS

General

Read operations are initiated by a Control tag (3) with Bus bit 1 true. This enables the analog data detection circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the read analog to digital converter which changes it into digital MFM data.

The read PLO and data separator change the MFM data to NRZ and also generate a 9.67 MHz Read Clock signal. Both data and clock are then sent to the controller.

The read circuits also detect the Address Mark area and send an Address Mark Found signal to the controller.

Figure 3-63 shows the main elements in the read circuits and table 3-7 briefly describes each of these elements. The following paragraphs further describe the read circuits.

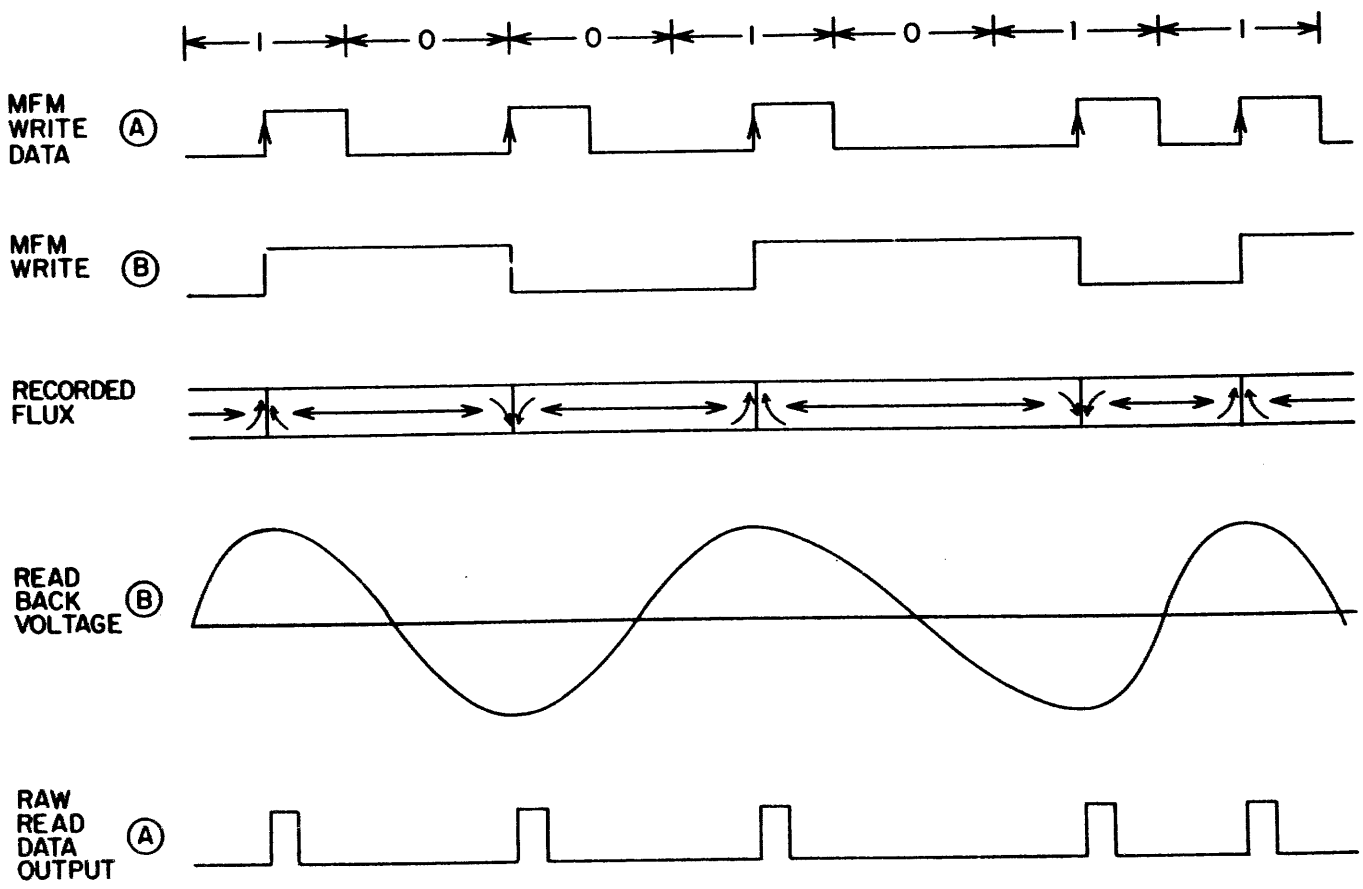


Figure 3-62. MFM Recording - Waveforms and Timing

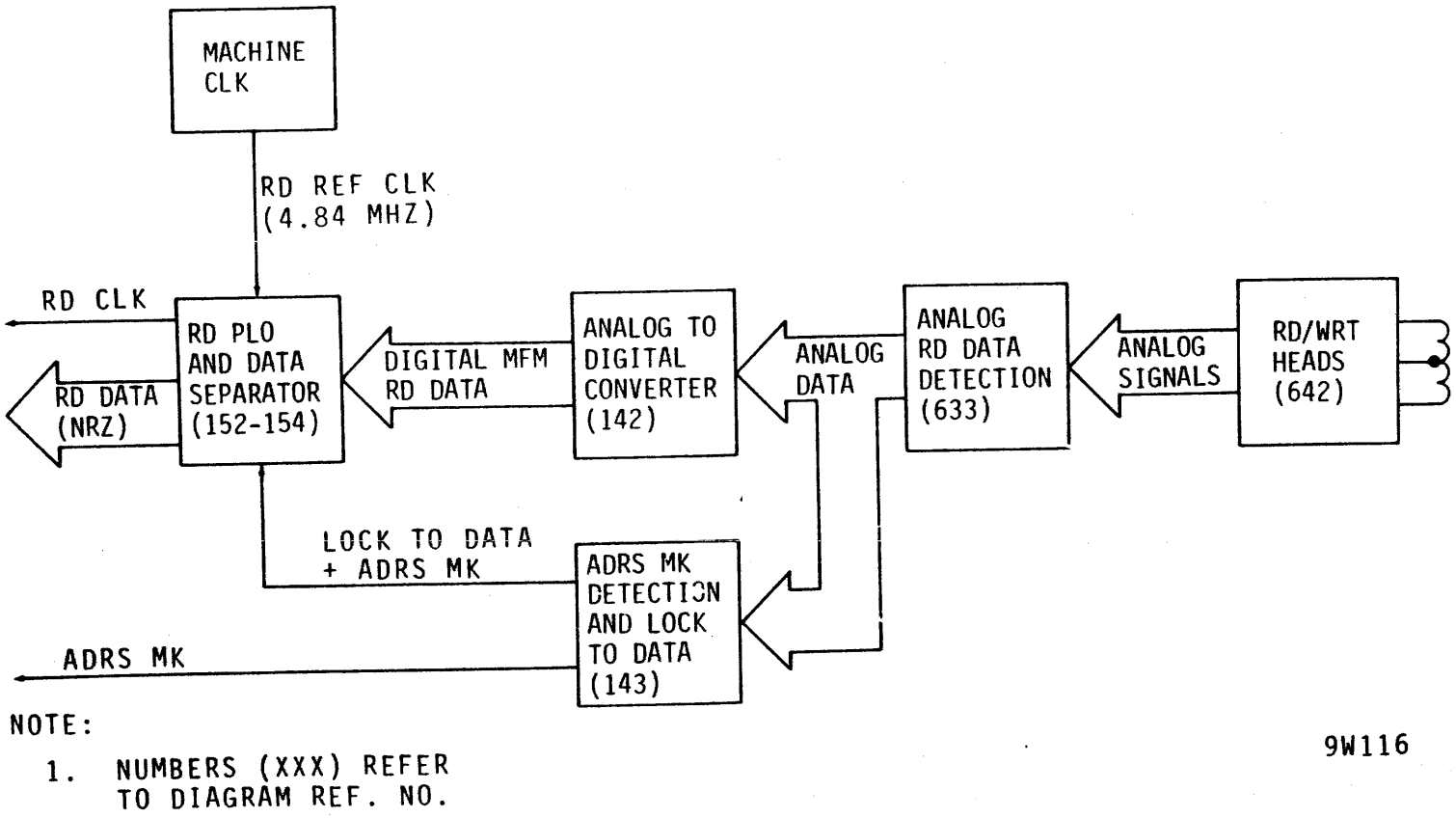


Figure 3-63. Read Circuits Block Diagram

TABLE 3-7. READ CIRCUIT FUNCTIONS

Circuit	Function
Analog Read Data Detection Circuits	Processes the analog signals sensed by the read/write heads so that they can be used by the digital to analog converter.
Digital to Analog Converter	Changes the analog MFM data to NRZ and also generates a 9.67 MHz Read Clock signal. It transmits both of these to the controller.
Address Mark Detection	Detects the Address Mark and transmits an Address Mark Found signal to the controller.

Analog Read Data Detection Circuits

The analog read data detection circuits (refer to figure 3-64) processes the analog MFM data detected from the disk so it can be used by the analog to digital converter circuits.

The Read Pre-amplifier provides preliminary amplification of the analog voltage induced in the read coil. This voltage is induced in the coil by the magnetic flux stored in the disk oxide during write operations (refer to discussion on Basic Read/Write Principles). The frequency of the magnetic field flux transitions sensed by the read coil.

The low pass filter on the output of the Read Pre-amplifier attenuates the high frequency noise on the read data signals and provides a linear phase response over the range of read data frequencies. The output of the filter is applied to the AGC amplifier. This circuit generates an output signal amplitude that remains within certain limits regardless of the amplitude of the input signal. The AGC Gain Control circuit provides the control voltage for the AGC amplifier and also provides inputs to the Address Mark detection circuits.

The Buffer amplifier processes the AGC amplifier output to provide the proper input for the analog to digital converter circuit.

Read Analog to Digital Converter

The read analog to digital converter circuits (refer to figure 3-65) receive analog detection circuit and convert it to digital MFM data.

The analog to digital converter circuit consists of high and low resolution channels and the Data Latch FF. The high and low resolution channels detect the analog data by means of zero cross detectors consisting of Schmitt triggers. The zero cross detectors convert the analaog data to digital pulses which are then applied to the Data Latch FF. The FF uses the outputs of both channels to produce a digital MFM data output. The low resolution channel provides the D input to the FF and the high resolution channel provides the clock. This produces an output from the Data Latch FF which retains the timing of the high resolution channel.

Both channels are necessary because of certain high frequency components present in the analog read data signals. These components can cause extraneous zero crossings which are detected by the zero cross detectors. However, the low pass filter in the low resolution channel attenuates the high frequency components thus eliminating any possible extraneous outputs from the channels zero crossing detector.

The high resolution channel still detects the crossings and generates clock inputs to the FF, but without the D input provided by the low resolution channel the extraneous clock pulses are ignored.

The digital MFM read data is sent to the PLO and data separator which use it to generate the NRZ data and Read clock.

Lock to Data and Address Mark Detection Circuits

These circuits generate (refer to figure 3-66 and 3-67) the Lock to Data signal and also detect the Address Mark area. The Lock to Data signal is used to synchronize the read PLO and data separator. The Address Mark signal is used to synchronize the read PLO and data separator and is also sent to the controller.

The Lock to Data signal is active whenever the Lock to Data one shot is in the set state. This one shot is triggered (to the set state) when either the Read Gate signal goes inactive or the Address Mark is detected.

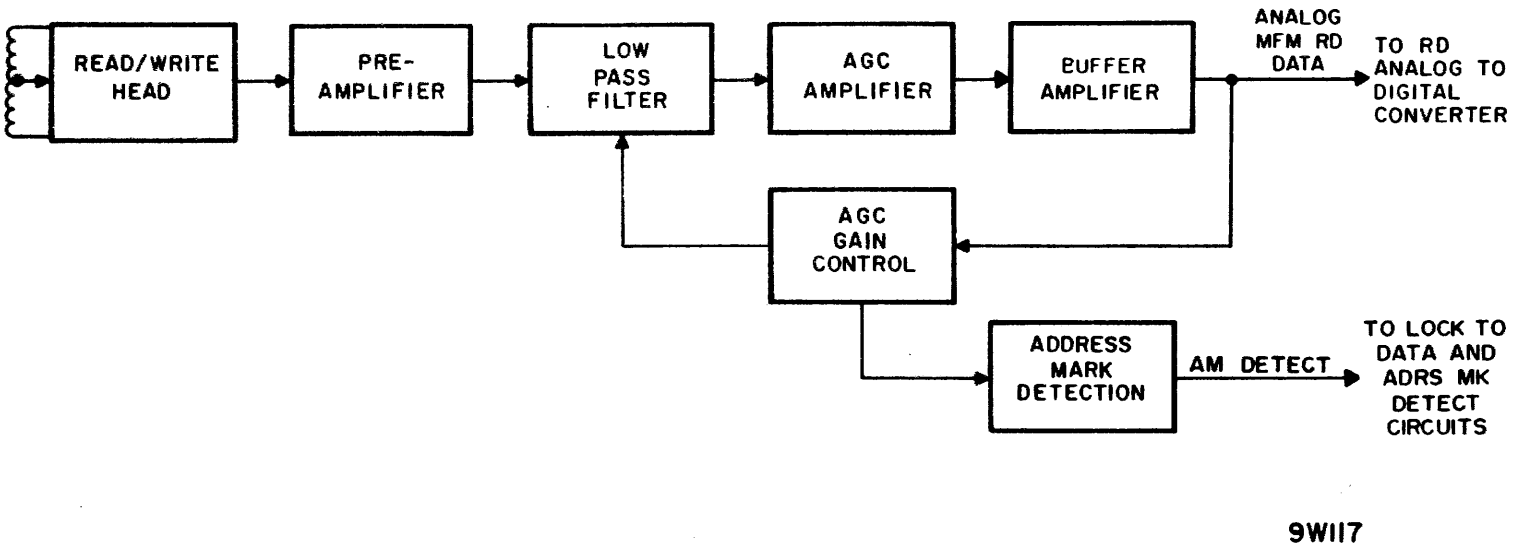


Figure 3-64. Analog Read Data Detection Circuits

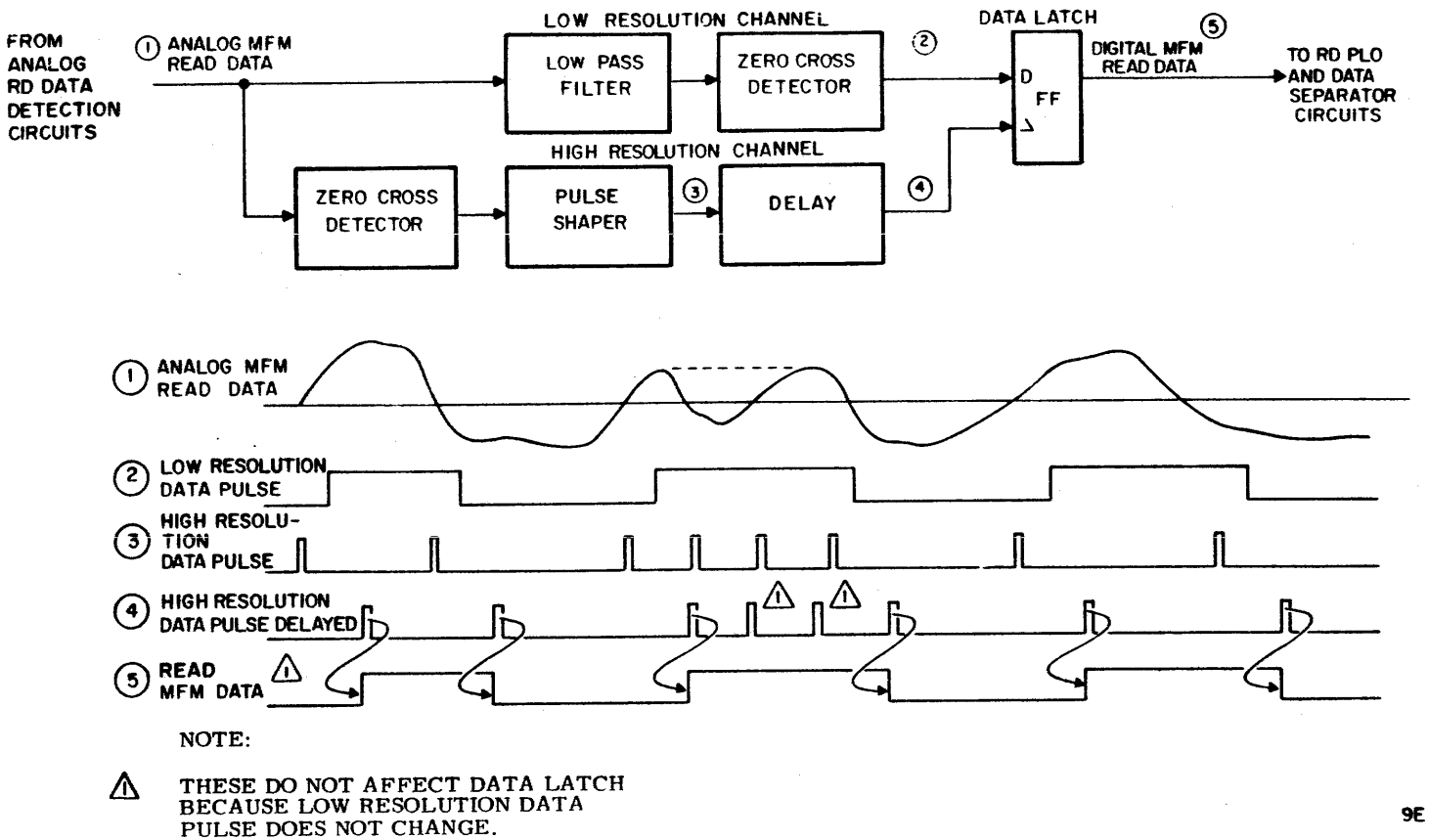


Figure 3-65. Read Analog To Digital Converter Logic and Timing

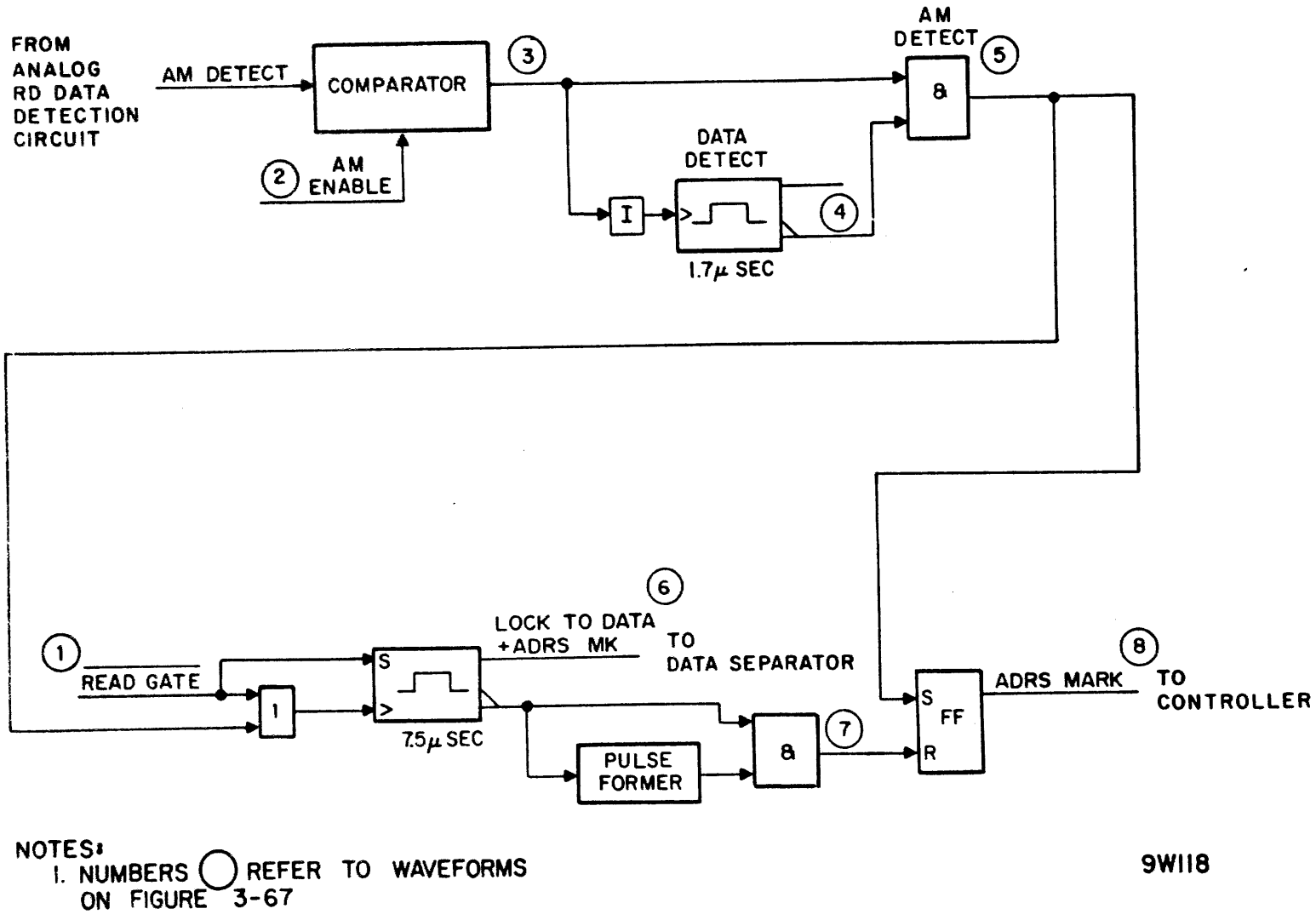


Figure 3-66. Lock to Data/Address Mark Detection

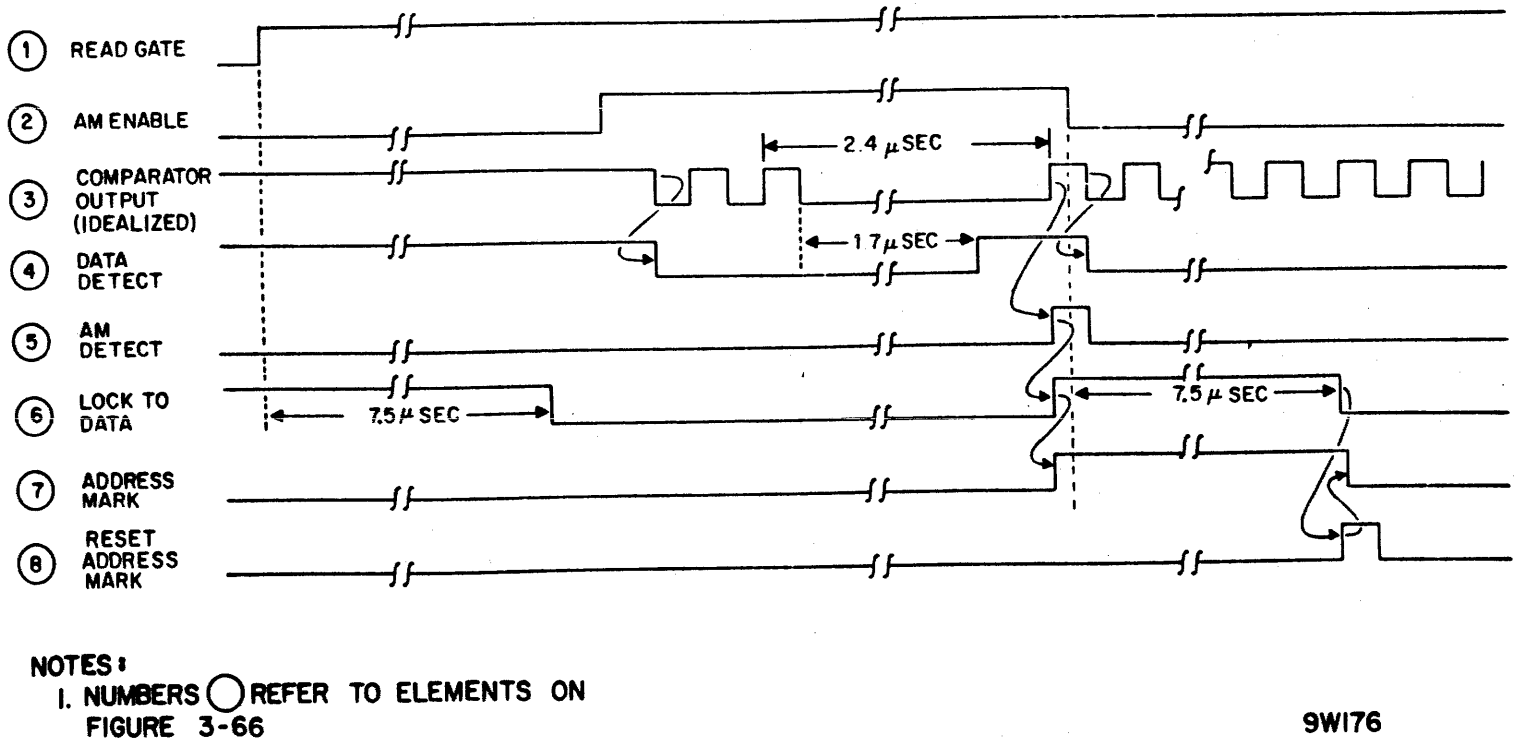


Figure 3-67. Lock to Data/Address Mark Detection Logic

When the Read Gate signal goes inactive it triggers the one shot and also causes it to be held in the set state. When the Read Gate signal goes active again, it removes the set conditions from the one shot and allows it to time out after 7.75 microseconds. Detecting the Address Mark also triggers a 7.75 microsecond pulse from the one shot. Therefore, a 7.75 microsecond lock to data period occurs at the beginning of every read operation and following every Address Mark area.

The Address Mark consists of an area about 2.4 microsecond in length that contains neither MFM ones or zeros. When the drive detects this area it generates a 7.75 microsecond Address Mark signal.

The address mark detection circuit is enabled only during read operations (Tag 3 and Bus bit 1 active). The controller activates the circuit by raising Bus bit 4 (Address Mark Enable).

The Address Mark Enable signal causes the comparator to start generating output pulses that trigger and retrigger the Data Detect one shot. The comparator generates the output pulses only when there are input data pulses. Therefore, during the Address Mark area the comparator stops generating pulses and the one shot times out 1.7 microsecond after the last data pulse was detected. The first data pulse following the Address Mark area enables the Address Mark Detect gate. This triggers the Lock to Data one shot which causes the 7.75 microsecond Lock to Data and Address Mark signals to be generated.

Read PLO and Data Separator

General

This circuit has two functions: (1) to convert the MFM data from the analog to digital converter into NRZ data and (2) to generate a Read Clock signal which is locked to the frequency of the read data (9.67 MHz nominal). Both the NRZ data and the Read Clock signal are transmitted to the controller.

The read PLO and data separator circuits consist of four main parts (refer to figure 3-68):

- Input Control - Controls whether MFM data or 4.84 MHz clock pulses will furnish the input to the circuit.
- Data Strobe Delay - Delays the pulses to provide the proper input to the VCO. These circuits also provide error recovery capability.

- Phase Lock Loop - Synchronizes the circuit outputs to the phase and frequency of the inputs.

- Data Separator - Converts the MFM data to NRZ data and generates the Read clock. This circuit is actually a part of the phase lock loop.

The remainder of this discussion further describes the read PLO and data separator circuits.

Input Control

The input control circuit (refer to figure 3-68) selects the input that will be used by the read PLO and data separator circuits. This input will always be either MFM data from the read analog to digital converter or 4.84 MHz clock pulses from the servo frequency multiplier circuit.

The 4.84 MHz clock signal is used only when the drive is not reading MFM data, such as before Read Gate is raised. It also uses the 4.84 MHz clock whenever the Address Mark Enable signal is active because this indicates the drive is expecting the Address Mark which contains no MFM data. The drive uses the clock signal as a substitute for the read data for two reasons: (1) the signal is derived from the track servo dibits and therefore, its frequency (like that of the read data) varies directly with disk pack speed and (2) after being processed by the pulse forming circuits, it has about the same nominal frequency as the read data (9.67 MHz). This results in it being easier for the phase lock loop to synchronize to the proper frequency when switching from one of the signals to the other.

Once selected the signal is applied to a pulse forming network which generates a 20 ns pulse for each transition of the input. These pulses are then applied to the data strobe delay circuits and also furnish the data input to the data separator.

Data Strobe Delay

The purpose of the data strobe delay circuit (refer to figure 3-68) is to delay the data pulses sufficiently to provide the proper timing relationship at the input to the phase lock loop. The output of the data strobe delay circuit is delayed by a time determined by the state of the Data Strobe Early and

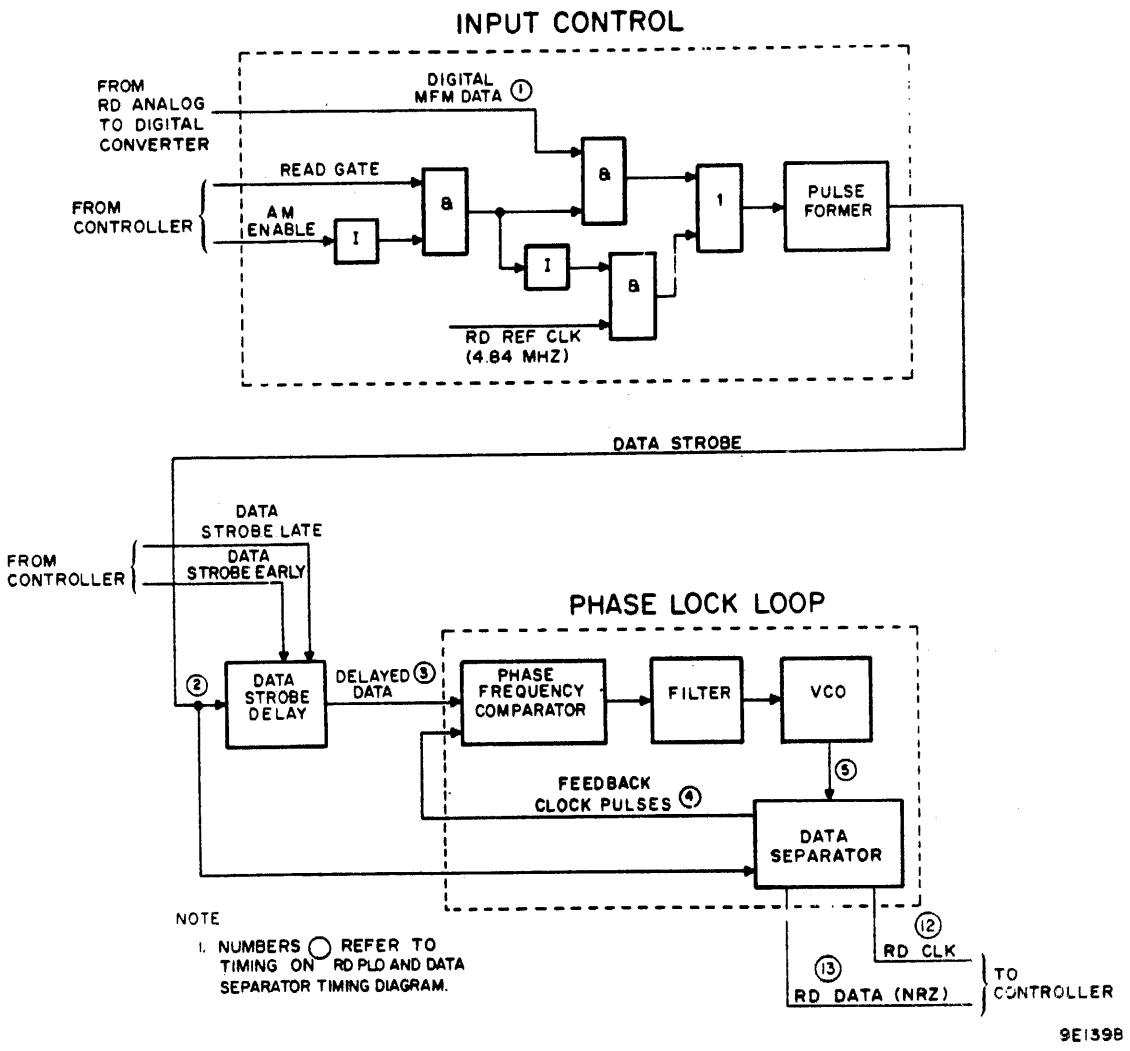


Figure 3-68. Read PLO and Data Separator Circuits

Data Strobe Late signals. These signals facilitate the recovery of marginal data and are enabled by Data Strobe Early or Late (Bus Bit 7 or 8) and Control Tag (3).

The output of this circuit is the Delayed Data signals which are sent to the input of the phase lock loop.

Phase Lock Loop

The phase lock loop (refer to figure 3-68) synchronizes the read PLO/data separator circuit outputs (NRZ data and Read Clock) to the input (either MFM data or 4.84 MHz clock). The loop accomplishes this by comparing and following two signals: (1) the Delayed Data signals which have a constant phase and frequency relationship to the input MFM data or 4.84 MHz Clock (whichever is used) and (2) the Feedback Clock Pulse signals which have a constant phase and frequency relationship to the output NRZ data and Read Clock signals. The loop inputs are applied to the phase/frequency comparator.

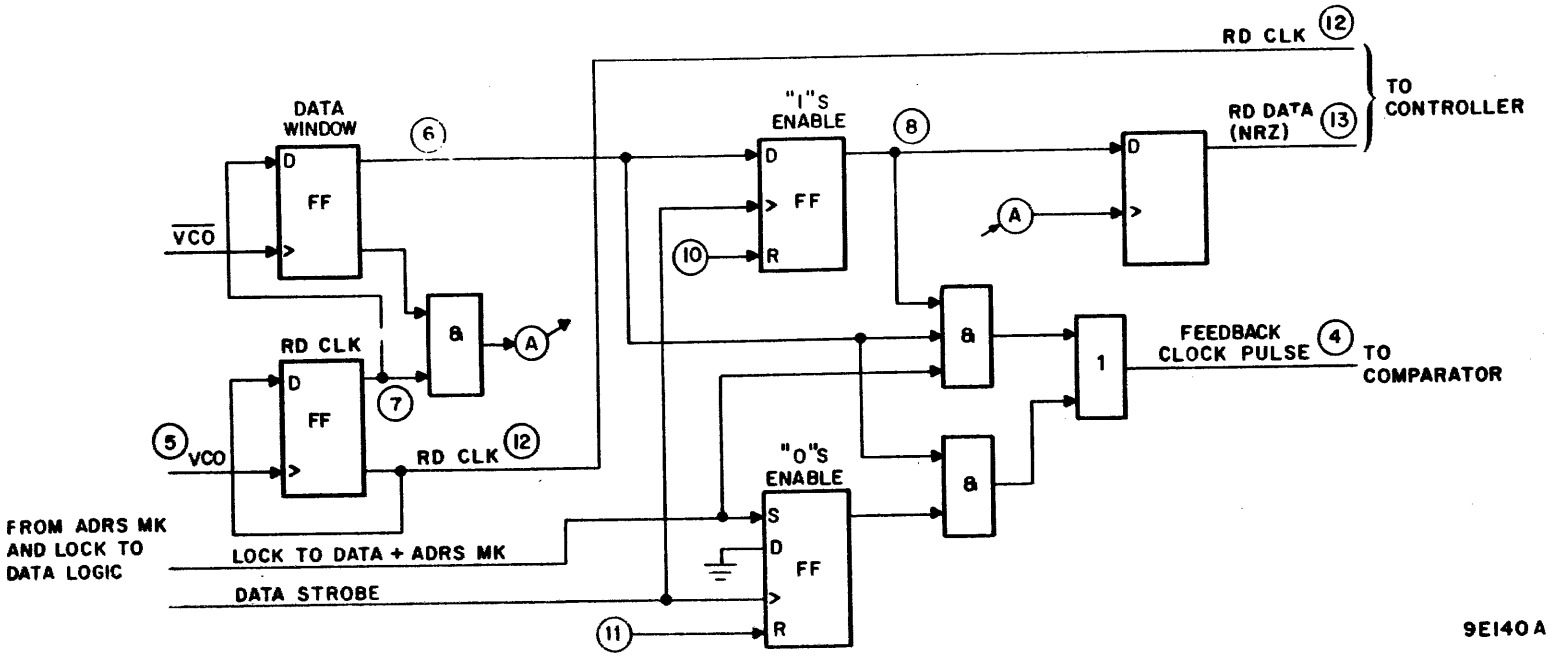
The phase/frequency comparator generates output pulses which are a function of the phase and frequency between the positive going edges of the inputs. The filter circuit uses the comparator outputs to generate a contol voltage for the voltage controlled oscillator (VCO).

This control voltage causes the frequency of the VCO to vary in the direction necessary to eliminate the phase and frequency differences between the two signals that were input to the comparator.

The output frequency of the VCO is actually twice that of the input so for an input of 9.67 MHz it has an output of 19.34 MHz. However, the data separator divides this by two before generating the Feedback Clock Pulse signals thereby providing a feedback to the comparator that satisfies the loop.

Data Separator

This circuit determines if the data pulses represent a one or zero and then converts the data to NRZ. It also generates the Feedback Clock Pulses to the comparator and the 9.67 MHz Read Clock that is sent to the controller. Figures 3-69 and 3-70 show simplified logic and timing for the data separator circuit.



NOTE

1. NUMBERS ◯ REFER TO TIMING ON RD PLO AND DATA SEPARATOR TIMING DIAGRAM.

Figure 3-69. Data Separator Logic

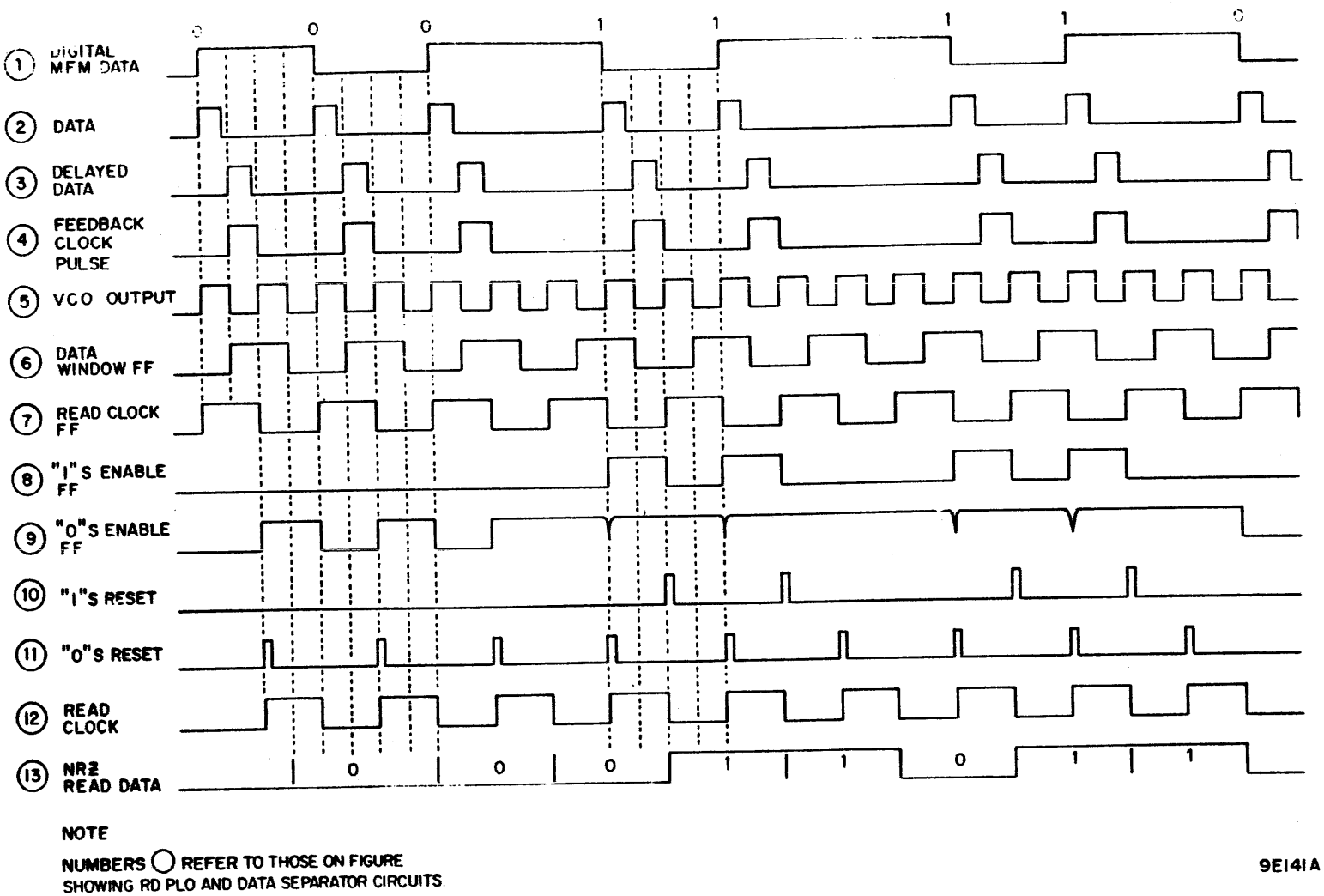


Figure 3-70. RD PLO and Data Separator Timing

The VCO outputs provide the proper timing relationships for the data separator by controlling the Data Window and Read Clock FFs. The Read Clock FF generates the 9.67 MHz Read Clock signal and also provides timing signals to the data separator logic. The Data Window FF generates the Data window which is used to determine whether the input data pulses represent ones or zeros. The actual decoding of the data is done by the "1's" Enable and "0's" Enable FFs.

If a data pulse represents a one it occurs during the data window and sets the "1's" Enable FF. Setting this FF generates a Feedback Clock pulse and causes the Data Buffer FF to generate a NRZ one.

If the data pulse represents a zero the "1's" Enable FF is not set and the Data Buffer FF generates a NRZ zero. In this case the "0's" Enable FF which is set by every data pulse generates the Feedback Clock Pulse signal.

Before accurate detection of data can begin, the proper phase relationship must be established between the data (representing ones and zeros) and the VCO output pulses. This is done during a 7.75 microsecond lock to data period which is initiated by the Lock to Data signal. This signal is a 7.75 microsecond pulse that occurs when the Address Mark is detected. The Lock to Data signal holds the "0's" Enable FF set and disables the output of the "1's" Enable FF. Therefore, if the circuit is to synchronize properly the pulse must occur during a period when the drive is reading only zeros.

WRITE CIRCUITS

General

The Write circuits operation is initiated by a Control tag (3) with Bus bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. The write data is received via the bidirectional Read/Write data line and is first sent to the RTZ to MFM coverter/write compensation circuits. These circuits convert the data to MFM and also compensate it for peak shift (refer to discussion on basic read/write principles for more concerning peak shift). The compensated data is then processed by the write drive circuits and written on the disk.

Figure 3-71 shows the write circuits and table 3-8 briefly explains their function.

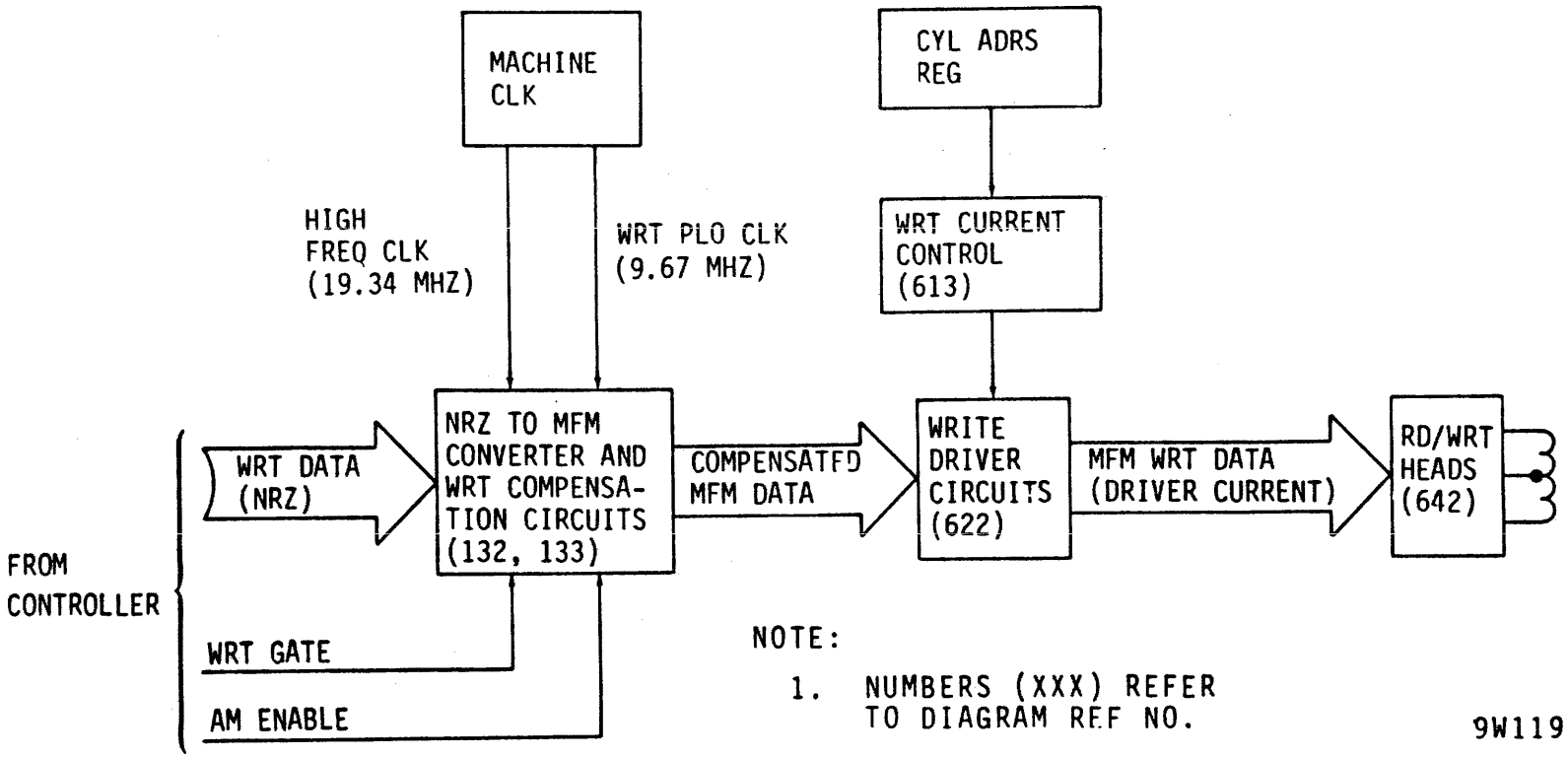


Figure 3-71. Write Circuits Block Diagram

TABLE 3-8. WRITE CIRCUIT FUNCTIONS

Circuit	Function
NRZ to MFM Converter and Write Compensation Circuits	Converts the NRZ data from the controller to MFM data and also compensates the data for problems caused by variations in the write data frequency.
Write Driver Circuits	Uses the MFM data to produce the current necessary to record data on the disk.
Write Current Control	Reduces the write current amplitude as the heads move from the outer tracks to inner tracks. This ensures that the correct amount of current will be used as the circumference of the cylinders decreases.

NRZ to MFM Converter/Write Compensation Circuits

The NRZ to MFM Converter/Write Compensation circuits convert the NRZ data into MFM data and also shift the output MFM pulses to compensate for peak shift (refer to discussion on basic read/write principles). Figures 3-72 and 3-73 show simplified logic and timing for these circuits.

The 9.67 MHz and 19.34 MHz signals from the servo frequency multiplier circuit provide basic timing signals for the write compensation circuits. The NRZ data from the controller provides the data input. These inputs are applied to the pattern decode and NRZ to MFM converter circuits.

The NRZ to MFM converter converts the NRZ data, into MFM data and applies it to a delay line. The delay line has three outputs which are combined with the outputs of the pattern decode logic (at the Early, Late and Nominal gates) to produce compensated write data.

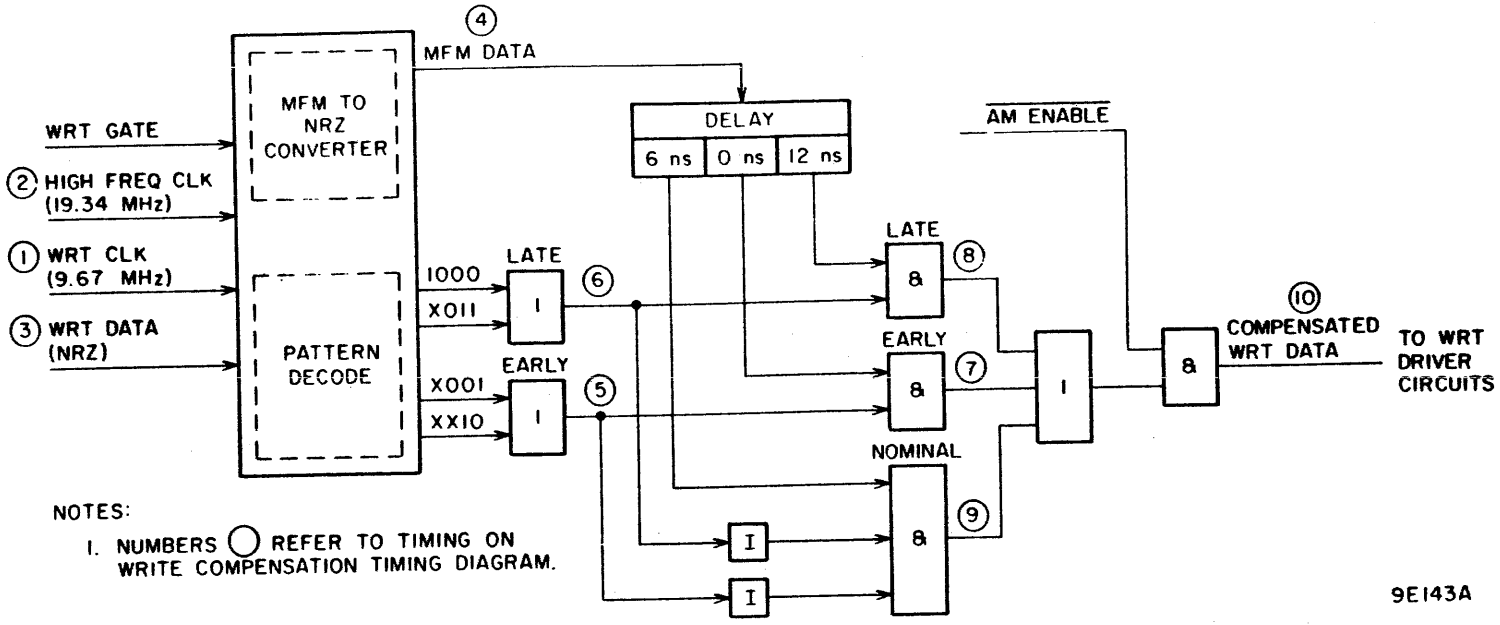


Figure 3-72. Write Compensation/NRZ to MFM Converter Circuits

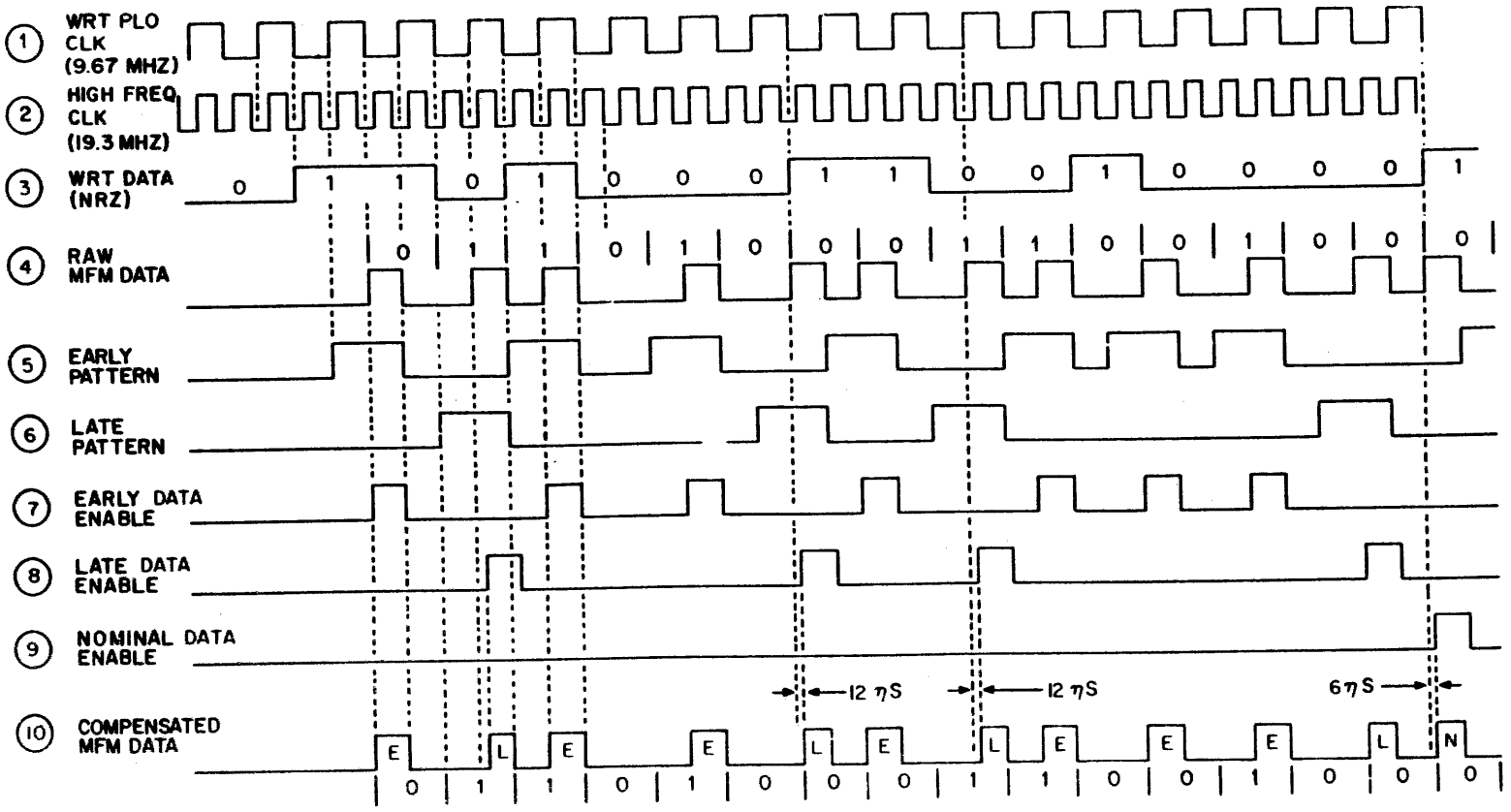


Figure 3-73. Write Compensation Timing

The pattern decode logic analyses the NRZ data and determines if its frequency is constant (00000 or 11111), increasing (011 or 1000), or decreasing (10 or 001). The outputs from the pattern decode logic enable either the Early, Late or Nominal gate (depending on the input frequency) to provide compensated Write data as follows:

- If frequency is constant, there will be no peak shift. In this case the data is defined as nominal and is delayed 6 ns.
- If frequency is decreasing, the apparent readback peak would occur later than nominal. To compensate for this, the data is not delayed and is therefore 6 ns earlier than the nominal data.
- If frequency is increasing, the apparent readback peak would occur earlier than nominal. Therefore, this data is delayed 12 ns which is 6 ns later than nominal.

After being write compensated the data is transmitted to the write driver circuits.

Write Driver Circuit

The compensated write data is sent to the read/write chassis and applied to a differential receiver in the write driver circuits (refer to figure 3-74). The output of the receiver then serves as a clock for the Write Toggle FF. This flip flop toggles only when the Write Enable signal is active. The output of this flip flop provide the input to the Write Driver which in turn generates the current for the read/write heads. The magnitude of the current applied to the heads is controlled by the write current control circuits.

Write Current Control

The magnitude of the write current sent to the heads is controlled as a function of cylinder address. This is referred to as write current zoning as the zones are divided into the following segments of tracks: 0-127, 128-255, 256-511, land 512 through 822. Write current is reduced at each zone boundary from outer to inner tracks.

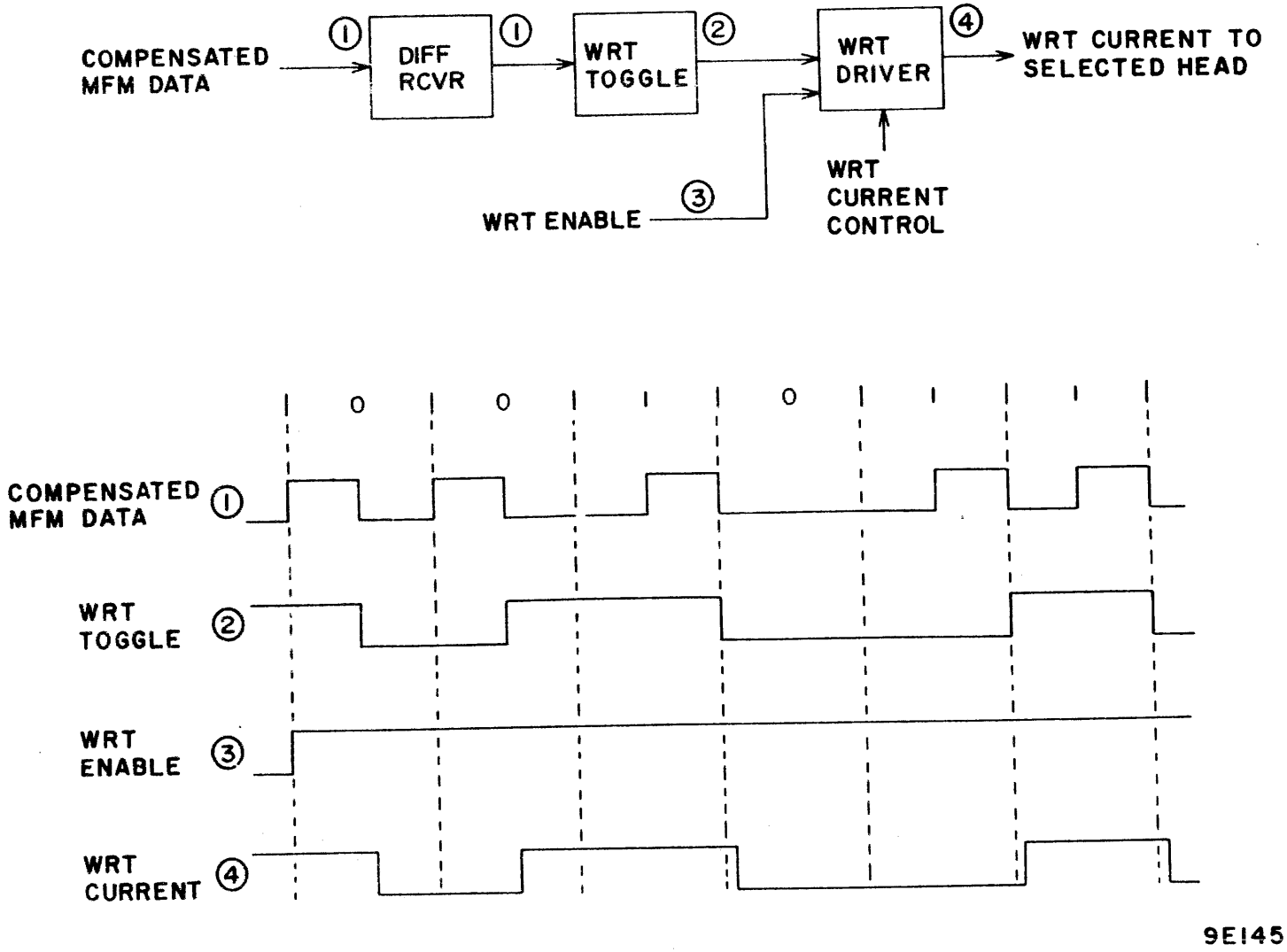


Figure 3-74. Write Driver Circuits and Timing

Write Data Protection

General

Write data protection consists of disabling the write driver circuit whenever there is danger of writing faulty data on the disk pack. It is initiated if the drive detects the Write Protect signal active, Fault latch set, or a low voltage condition. All of these are described in the following.

Write Protect

The Write Protect signal goes active if any of the following occurs.

- Controller commands a write while the heads are in an offset position (refer to discussion on Direct Seek Fine Position Control-Track Following).
- WRITE PROTECT switch on drive operator panel has been depressed to light the indicator. In this case, depressing the switch to extinguish the indicator causes the Write Protect signal to go inactive.
- Head alignment is being performed.
- Low dc voltage condition is detected or the disk pack speed slows down below 2700 r/min. Both of these conditions will also cause an emergency retract of the heads (refer to discussion on (Emergency Retract).

Fault

The Fault latch sets as a result of a number of drive malfunctions. The conditions causing the Fault latch to set are described in the discussion on Fault and Error Conditions.

Loss of Voltage

If power is lost or drops below a certain level, an emergency retract is performed. However, in this case it is possible that other signals used to disable the write driver (Write Protect and Fault) will not function properly and the drive will continue to write while the heads are being retracted. This could alter or destroy data already on the pack. The loss of voltage protection circuit consists of a capacitive discharge network that ensures the write circuits are disabled until the heads are unloaded.

FAULT AND ERROR CONDITIONS

GENERAL

The following describes those conditions which are interpreted by the drive as errors. All of these conditions either light an indicator at the drive and/or send a signal to the controller indicating an error has occurred.

These errors are divided into two categories: (1) those indicated by Fault Latch and register (2) those not indicated by Fault Latch and register. Both are explained in the following (refer to figure 3-75).

ERRORS INDICATED BY FAULT LATCH AND REGISTER

General

Certain errors set the drives Fault latch and also set the fault register latches associated with the error condition.

Setting the Fault Latch does four things (1) enables the fault line to the controller (2) lights the FAULT indicator on the drives operator control panel (3) clears the drives Unit Ready signal (4) inhibits the drives write and load circuitry. These events prevent further drive operations from being performed until the error is corrected and the Fault latch is cleared.

Providing the error condition or conditions no longer exist, the Fault latch is cleared by any of the following:

- FAULT switch on operator panel.
- Controller Fault Clear signal from the controller.
- Initialize signal from the controller.
- Maintenance Fault Clear switch on Fault card.
- Powering down the unit.

Whenever an error occurs that sets the Fault latch, it also sets a latch in the fault register. These latches provide a means of storing the error indication unit so it can be referred to later for maintenance purposes. The fault register latches are cleared only by powering down the drive or by the Maintenance Fault Clear switch on the fault card.

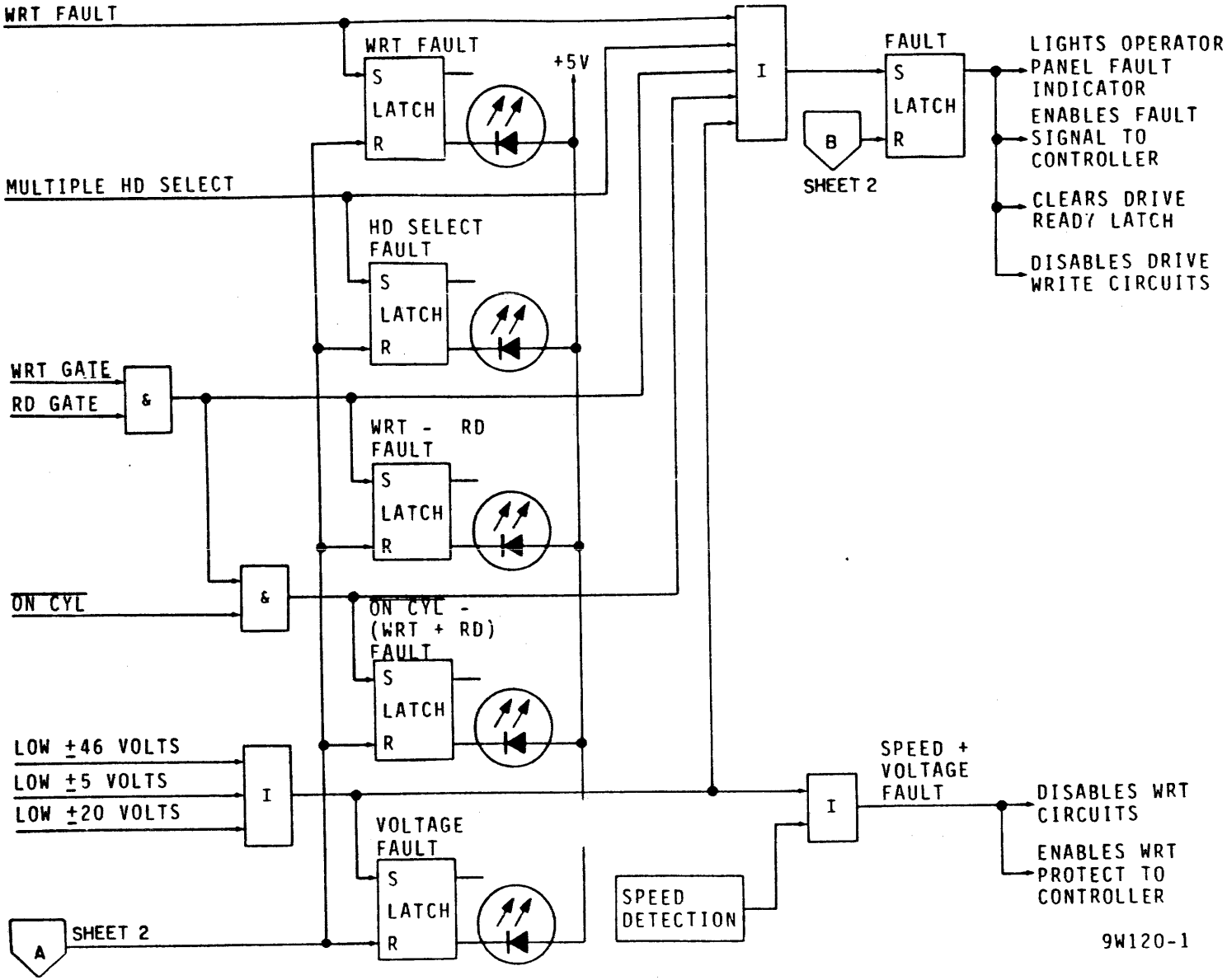


Figure 3-75. Fault and Error Detection Logic (Sheet 1 of 2)

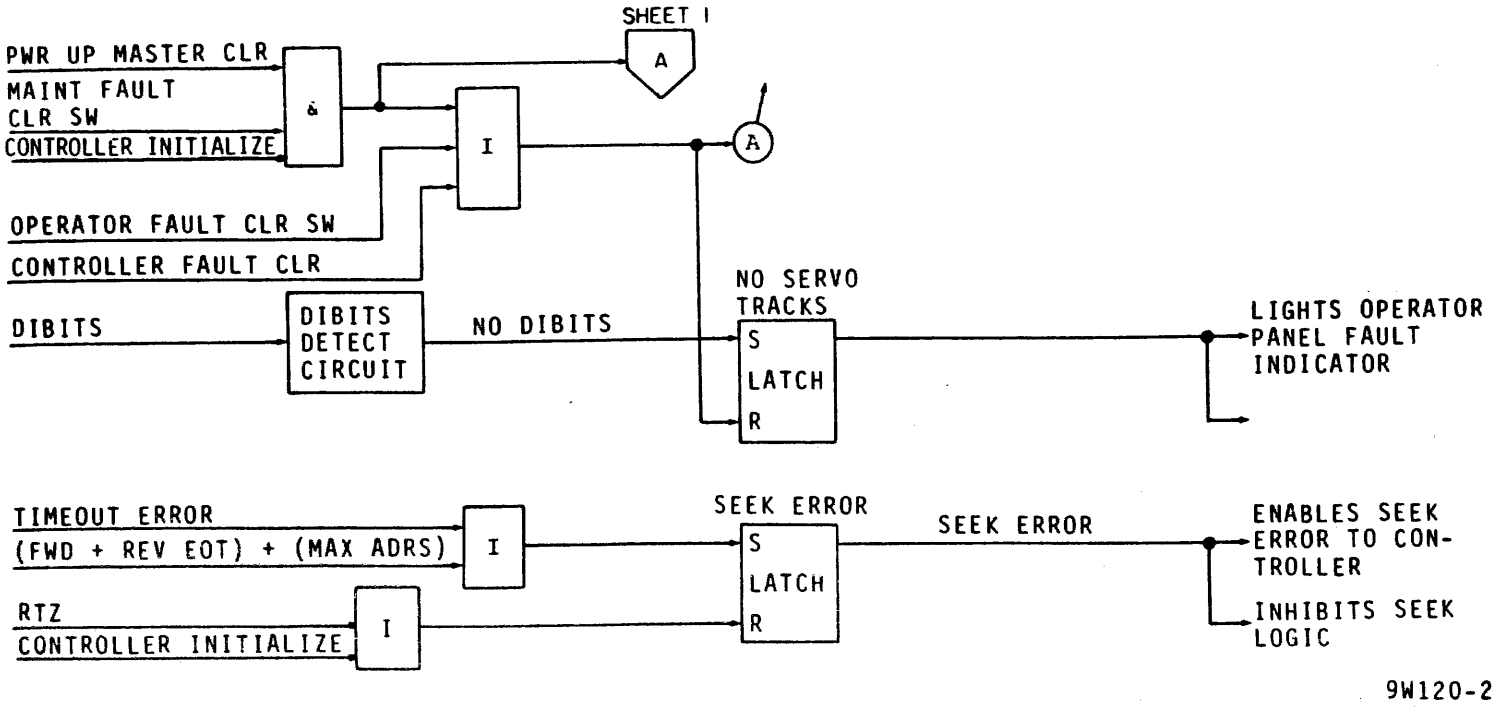


Figure 3-75. Fault and Error Detection Logic (Sheet 2)

The following describes each of the conditions causing the Fault latch and fault register latches to be set.

Write Fault

A write fault is indicated if any of the following conditions exist.

- Low output from write driver indicating it may not be operating properly.
- Low current input to write driver.
- Low +22 volts to write driver.
- No write data transitions when Write Gate is active.

More Than One Head Selected

This fault is generated whenever more than one head is selected. The outputs of the head select circuits are monitored by summing and voltage comparator circuits. If more than one head is selected, the circuit generates a Multiple Select Fault.

Read and Write

This fault is generated whenever the drive receives a Read gate and Write gate simultaneously from the controller.

(Read or Write) and Off Cylinder

This fault is generated if the drive is in an Off Cylinder condition and it receives a Read or Write gate from the controller.

Voltage Fault

This fault is generated whenever the ±46, ±5 or ±20 voltages are below satisfactory operating levels.

ERRORS NOT INDICATED BY FAULT LATCH OR REGISTER

General

The following errors are detected by the drive but are not stored in the fault register and do not set the Fault latch. However, they do sense the drive to give other error indications and this is explained in the following paragraphs

Low Speed or Voltage

The Speed or Voltage Fault signal goes true when the drive detects either a low voltage condition or that drive spindle speed is below 2700 r/min. When either of these are detected, the drive write circuits are disabled and the Write Protect signal is sent to the controller. These also result in an emergency retract of the heads (refer to discussion on Emergency Retract).

No Servo Tracks Fault

If dibits are not detected within 350 ms after the load seek sequence begins, the No Servo Tracks latch is set. This lights the FAULT indicator on the drive operator control panel and also enables the Return to Zero (RTZS) logic. Enabling the RTZS logic causes the heads to unload. Another load cannot be started until the No Servo Tracks latch is cleared. The No Servo Tracks latch is cleared in the same manner as the Fault latch.

Seek Error

The Seek Error latch is set by any of the following error conditions:

- On Cylinder was not obtained within 500 ms from the start of the seek.
- Forward or reverse end of travel (EOT) sensed.
- Drive is commanded to seek to a cylinder address greater than 822.

Setting the Seek Error latch enables the Seek Error line to the controller and also inhibits the drive from performing another seek until the Seek Error latch is cleared. The latch is cleared by a Return to Zero Seek command.

MICROCIRCUITS

SECTION 4

INTRODUCTION

This section provides a functional understanding of the various microcircuits (integrated circuits or ICs) used in the equipment, including their MIL STD 806 (B/C) symbols as depicted in each logic diagram set. The section divides into three subsections each of which is described in the following paragraphs.

Section 4A discusses the characteristics, operational theory, and physical packaging of the TTL (transistor-transistor logic), ECL (emitter-coupled logic), and CMOS (complementary metal oxide semiconductor) microcircuit families. It concludes with some general information on operational amplifiers.

Section 4B describes the symbology used on the individual data sheets in section 4C, including the meanings of the various modifiers and qualifiers that are part of each logic symbol.

Section 4C contains the data sheets, arranged numerically by CDC element identifier, and information regarding data sheet interpretation.

GENERAL THEORY

SECTION 4A

INTRODUCTION

A microcircuit is an electronic circuit in a miniature package that performs a specific binary or linear function. Microcircuit complexity varies from a few logic gates to more than 100 gates on a single silicon chip. The term small-scale integration (SSI) is sometimes used to refer to a level of complexity of up to 12 logic gates. Medium scale integration (MSI) refers to circuits containing from 13 to 100 gates. Large scale integration (LSI) generally indicates circuits containing 100 or more gates. These gates may be interconnected within a microcircuit to form flip-flops, multivibrators, etc., which in turn are further interconnected, again within an individual microcircuit, to form registers, counters, coders/decoders, multiplexers/demultiplexers, etc. Thus it is possible for a microcircuit to provide simple gating functions (AND, OR, NAND, NOR) as in SSI, or to provide complex functions (registers, counters, arithmetic logic units, memories, etc.) as in LSI.

TRANSISTOR-TRANSISTOR-LOGIC (TTL)

TTL microcircuits provide small physical size and high performance-to-cost ratio. Reliability also improves because relatively few interconnections are necessary. Most TTL microcircuits are of the monolithic type. That is, a complete circuit or group of circuits is fabricated on a single silicon chip. Another type of microcircuit is the hybrid. Hybrid circuits consist of small discrete components mounted on a ceramic substrate. A metallization pattern on the substrate forms the interconnections. Hybrid circuits usually appear in relatively small quantities. Ordinarily, microcircuits cannot be opened for repair or troubleshooting.

STANDARD TTL CHARACTERISTICS

There are five series of TTL circuits: Standard, Low-Power, High-Speed, Schottky-Clamped and Low-Power Schottky TTL circuits. These series are functionally identical except for propagation time and power consumption. All five series are compatible; circuits from any series can interface with any other series. These series are described under their individual headings further in this section. A circuit of a series normally drives 10 circuits of the same series. However, combining circuits of different series varies the output drive capability (fan-out) from 1 to over 50. Typical values of the essential characteristics for all series are:

	Min	Nom	Max
Supply voltage	+4.75	+5.0	+5.25
High output voltage	+2.4	+3.3	
Low output voltage		+0.2	+0.4
High input voltage	+2.0	+3.3	
Low input voltage		+0.2	+0.8

The logic levels may be observed as indicated below, depending on the circuit load:

HIGH - from +2.0 to +3.3 volts.

LOW - from +0.2 to +0.8 volts.

TRI-LEVEL CIRCUITS

Tri-Level (tristate) circuits are similar to conventional TTL circuits. In addition to the normal high or low, tri-level circuits have a special control input that places the output of the circuit into an "off" (high impedance) state. In the off state, the circuit effectively disconnects from the output line. This characteristic is useful in a bus or party-line application where a number of driving circuits connect to a common transmission line, but only one circuit is active at any given time. A trilevel circuit draws significantly less input current when it is in the "off" state.

OPEN COLLECTOR CIRCUITS AND WIRED LOGIC

Some TTL microcircuits have an open-collector output. That is, the collector load or active pull-up portion of the output is not present. The output pin of the package connects only to the collector of an npn transistor. An open-collector output can go low only. It cannot drive the input of a following circuit high. To operate properly, an open-collector output must connect to an external pull-up resistor tied to Vcc.

More than one open-collector output may connect to the same pull-up resistor to form wired logic. This is sometimes called "collector dotting". Figure 4-1 illustrates open-collector circuits and a wired - AND gate. Each gate accomplishes the NAND operation for active-high inputs, and the NOR operation for active-low inputs. The expression for the function performed at the wired output is $Y = \overline{AB+CD}$ or $Y = \overline{AB+CD}$. Although sometimes referred to as "wired - OR" or "dot - OR", "wired - AND" is the correct description of the logic performed by this circuit.

UNUSED INPUTS

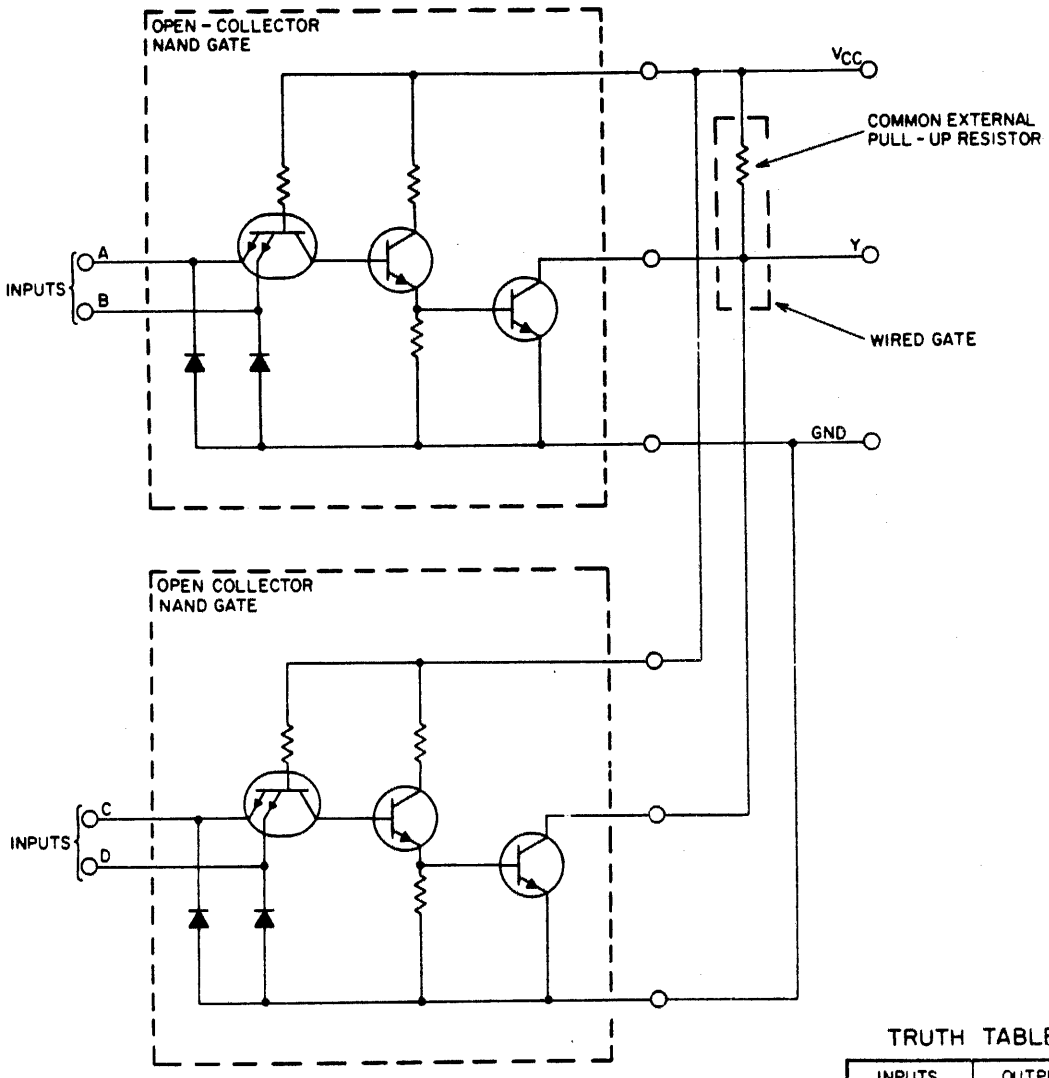
Generally unused inputs of TTL microcircuits are terminated in one of the following methods:

- Unused inputs are connected to used inputs if this does not exceed the fan-out of the driving output.
- Unused inputs are connected to Vcc through a 1 kΩ resistor. The resistor protects the input from transients. Up to 25 inputs may be connected to one 1 kΩ resistor.
- Unused inputs are connected to the output of an unused gate. This output must always be high.
- Unused inputs are connected to a separate supply voltage between 2.4 V and 3 V.

Leaving unused inputs open degrades the switching and noise characteristics of TTL microcircuits.

DUALITY OF FUNCTION

Figure 4-2 shows the four basic TTL gates (NAND, NOR, AND, OR). As implied by the logic symbols and truth tables, each of the two inverting gates may be considered as performing either the NAND function or the NOR function, depending upon which of



TRUTH TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H

X = IRRELEVANT

9K I A

Figure 4-1. Open-Collector Circuits and a Wired AND

the input states (high- or low-level) is regarded as being more significant -- that is, "active". Likewise, the two non-inverting gates can perform either the AND or the OR function, depending upon the polarity of the active inputs.

This principal of duality applies to all of the microcircuit families, not just to TTL. Later in this manual, these symbols are used in either representation to illustrate the logical construction of more complex circuits. When each of these composite circuits is constructed, a new symbol is generated. These symbols are then used to construct yet a more complex circuit, such as flip-flops being used to construct registers, counters, etc.

BASIC TTL CIRCUITS

Generally, all TTL microcircuits are drived by using combinations of the four basic (or "standard") gates shown on figure 4-2. These standard gates may be modified in various ways to meet the requirements for faster switching speed or lower power consumption. The several "series" thus produced are differentiated as follows:

- XXX = Standard series
- XXXL = Low-Power series
- XXXH = High-Speed series
- XXXS = Schottky Clamped series
- XXXLS = Low-Power Schottky series

The following paragraphs describe the characteristics of each series. Electrical schematic diagrams are included to show how the standard NAND gate (depicted at the top of figure 4-2) is modified for each series. The other basic gate types would, of course, undergo similar alterations.

Standard Series

Because of the effect of capacity, decreasing the impedance of a circuit tends to make the circuit switch faster. However, decreasing the circuit impedance also tends to increase power consumption. The Standard Series TTL attempts to compromise speed and power requirements. Typical switching speed is 10 ns. Power consumption is 10 mW per gate. The standard-series NAND gate, shown at the top of figure 4-2, operates as follows: If one or both inputs are low, Q1 conducts, bringing the

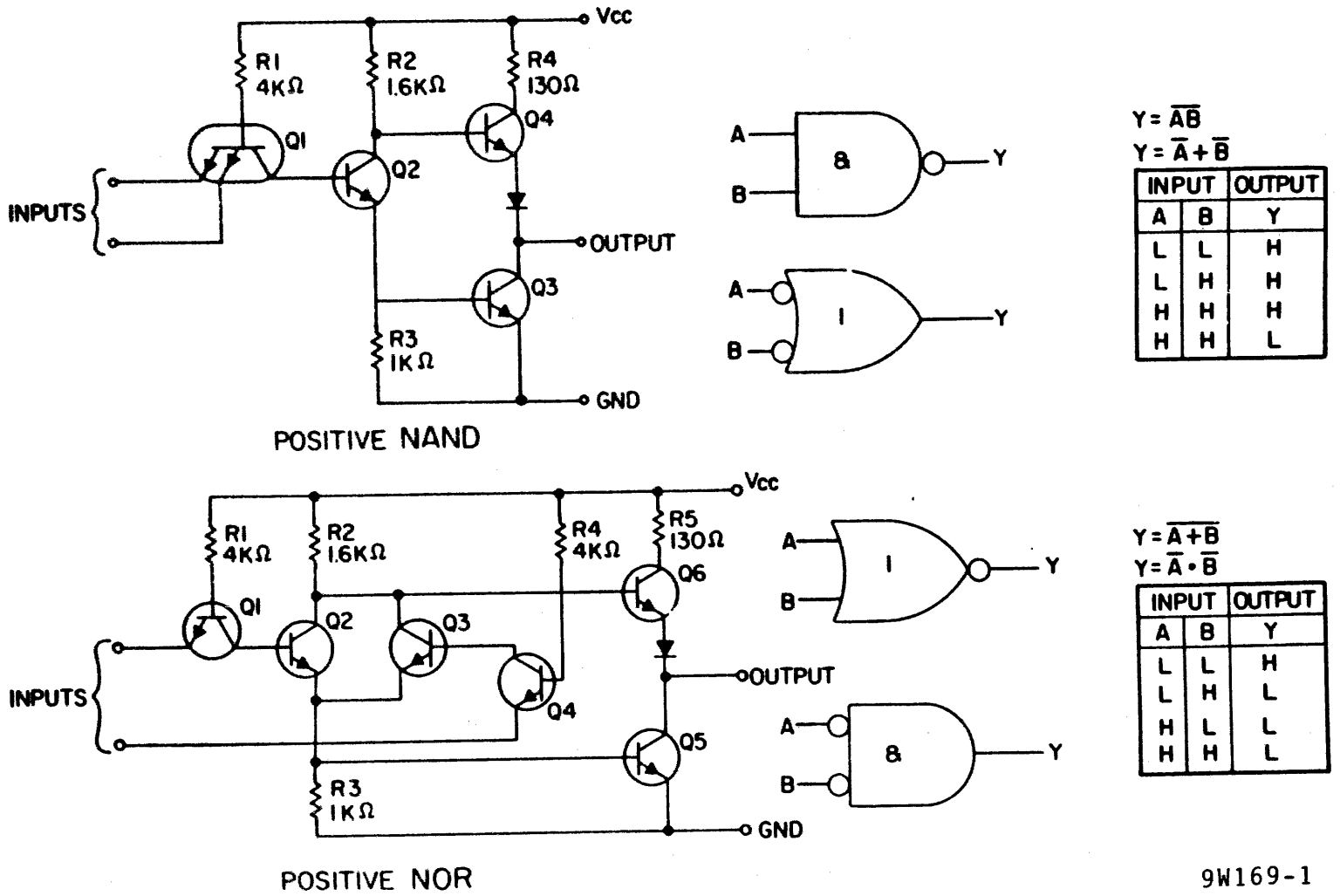


Figure 4-2. Basic TTL Gates (Sheet 1 of 2)

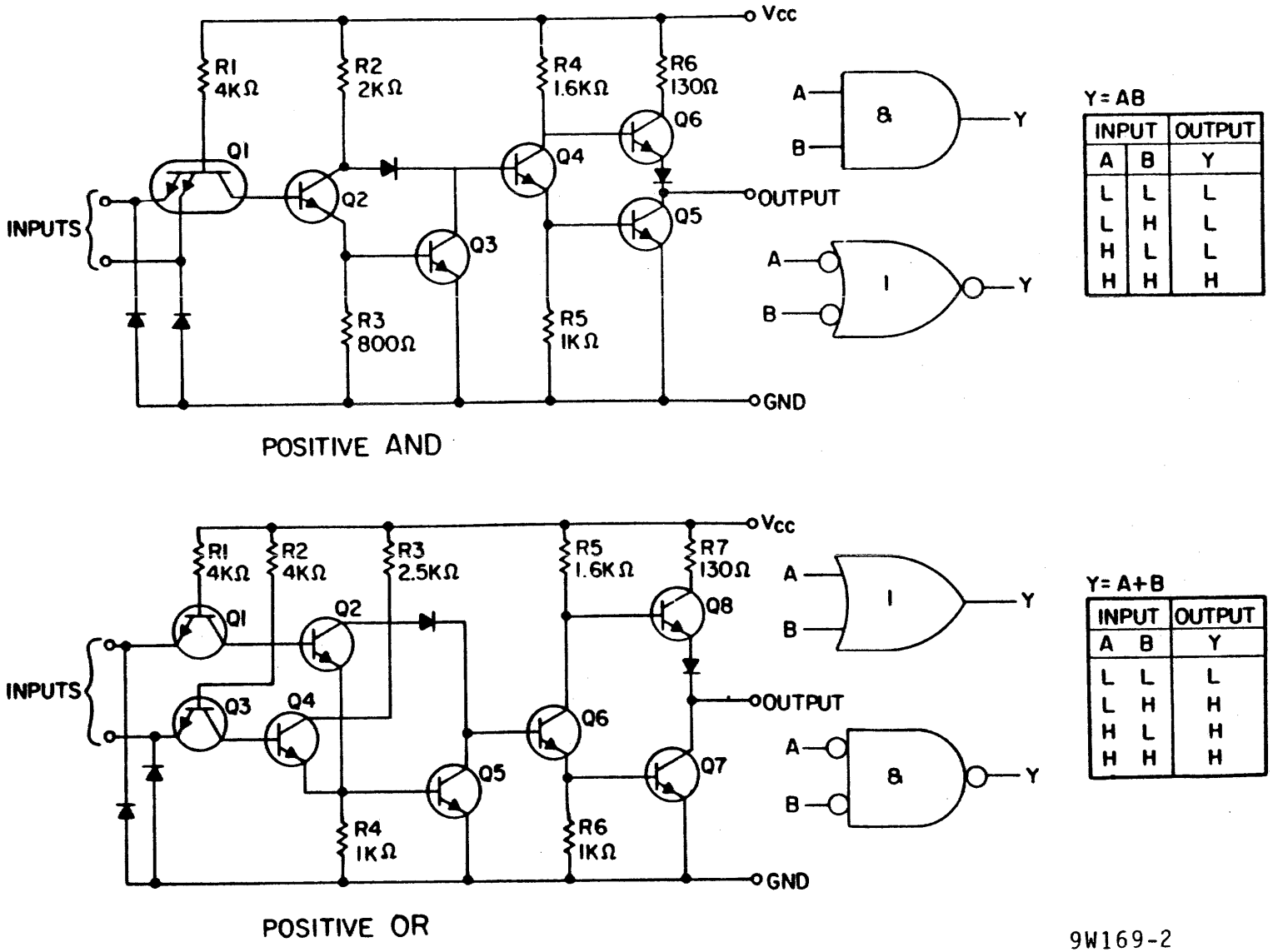


Figure 4-2. Basic TTL Gates (Sheet 2)

base voltage of Q2 close to ground. Q2 turns off, causing Q3 to be off and Q4 to be on. Thus, the output is high. If both inputs are high, the base-collector junction of Q1 is forward biased. This allows current to flow through R1 into the base of Q2 turning Q2 on. When Q2 is on, base current flows into Q3, and it turns on, causing the output to be low.

The multiple-emitter input transistor, Q1, replaces combinations of resistors, diodes, and transistors found in other types of logic. This configuration results in smaller size, which reduces stray capacity. Low stray capacity and low circuit impedances help to increase switching speed. At the output, Q3 and Q4 form an active pull-up or totem pole drive circuit. When the output is low, Q3 is saturated, providing a low source impedance. If the output is high, Q4 acts as an emitter-follower that also provides a low source impedance. This arrangement permits driving several loads and reduces the effect of capacity on switching time.

Low-Power Series

The low-power gate circuit is shown in figure 4-3. Typical switching speed is 33 ns, and power consumption is 1 mW per gate. Generally, an L suffix on the element identifier number indicates the low-power series.

High-Speed Series

Figure 4-4 shows the basic high-speed gate. Typical switching speed is 6 ns. Power consumption is 22 mW per gate. Usually, an H suffix on the element identifier indicates the high-speed series.

Schottky Clamped Series

Figure 4-5 shows the basic Schottky series gate. This series uses Schottky-barrier diodes as base-collector clamps. Clamping the collector prevents a transistor from saturating and thereby improves switching time. Switching time is 3 ns and power dissipation is 20 mW per gate. An S suffix on the element identifier indicates the Schottky series.

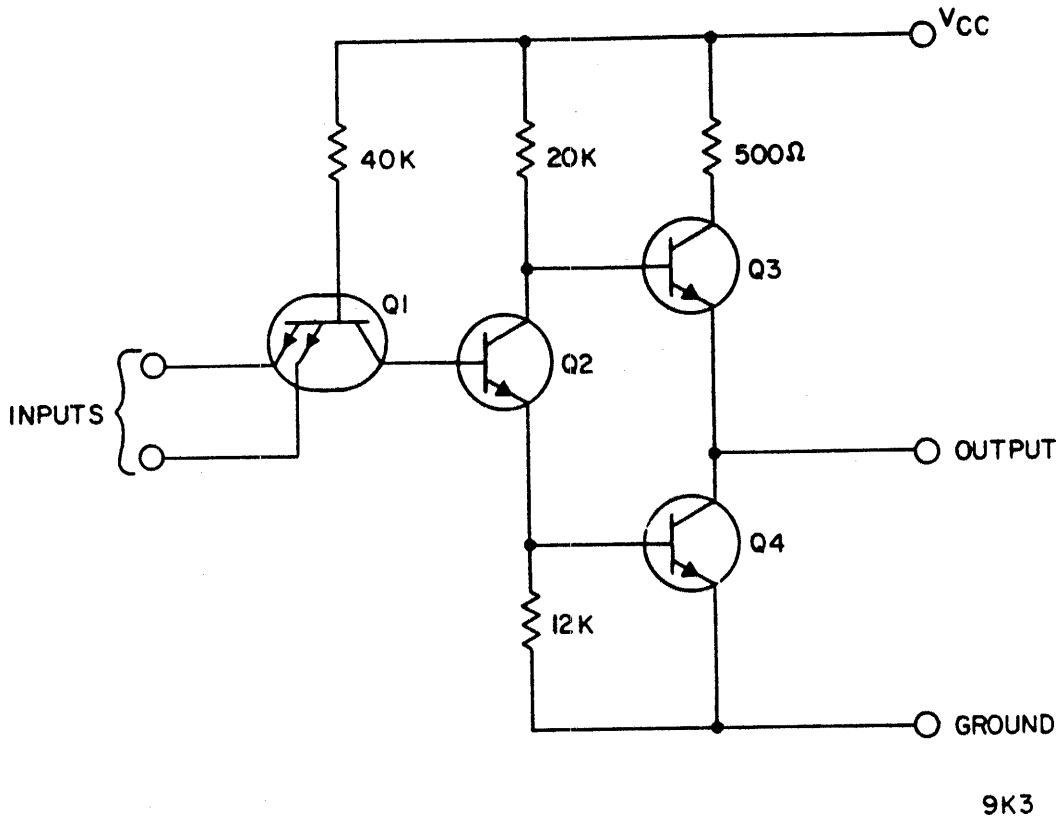


Figure 4-3. TTL NAND Circuit, Low-Power Series

Low-Power Schottky Series

The low-power Schottky gate is shown in figure 4-6. The suffix letters LS on the element identifier denote this series of microcircuit. The LS series offers a happy substitute for the standard TTL microcircuits, and in fact enjoys the best speed-power product of any of the five TTL series. Switching time is typically 9.5 ns per gate (as against 10 ns for the standard series), while power dissipation is 2 mW per gate as opposed to 10 mW for the standard TTL gate.

LOGIC INTERFACE CIRCUITS

Special microcircuits are used to interface different families of microcircuits. In the case of interfacing TTL (logic levels of HIGH = +3.3 volts, LOW = +0.2 volt) to ECL (logic levels of HIGH = -0.5 volt, LOW = 1.75 volts), circuits such as those illustrated in figure 4-7 are used.

TTL PACKAGING

TTL microcircuits are manufactured in several physical configurations. Three common ones are the dual-in-line packages, flat packages, and plug-in packages. These units are hermetically sealed and have from 8 to 40 pins. Flat packages and plug-in packages are available with various numbers of leads. Figure 4-8 shows an example of each package.

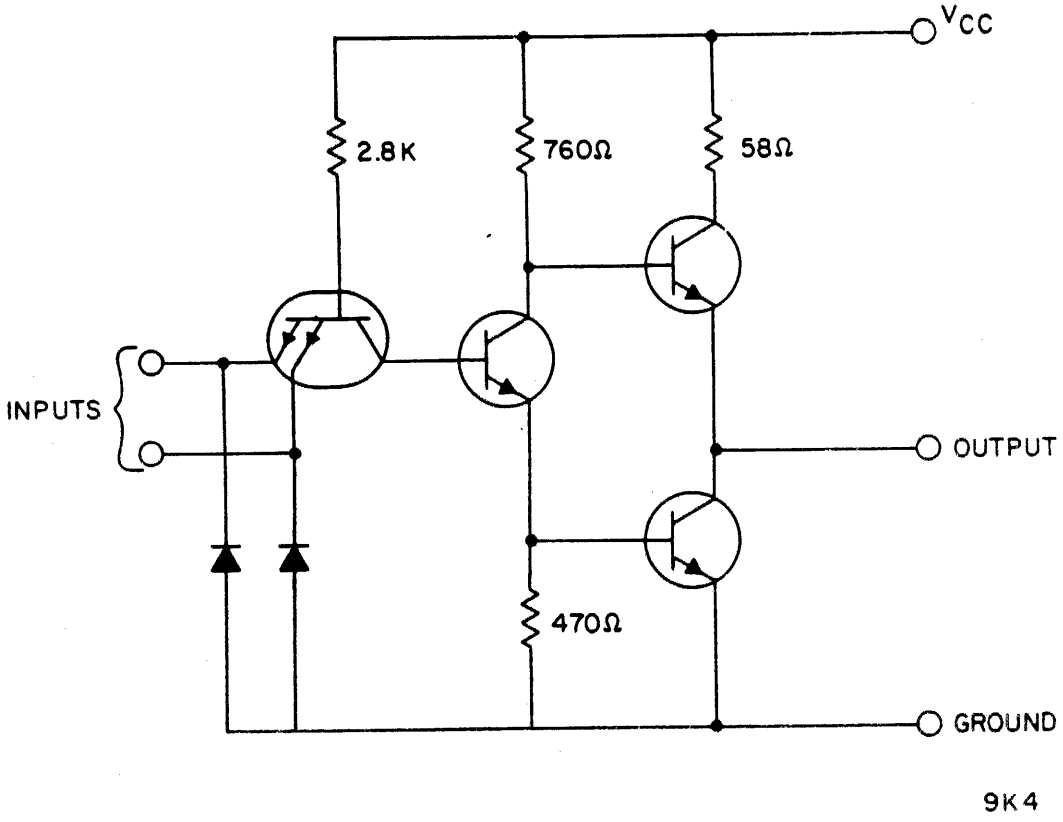


Figure 4-4. TTL NAND Circuit, High-Speed Series

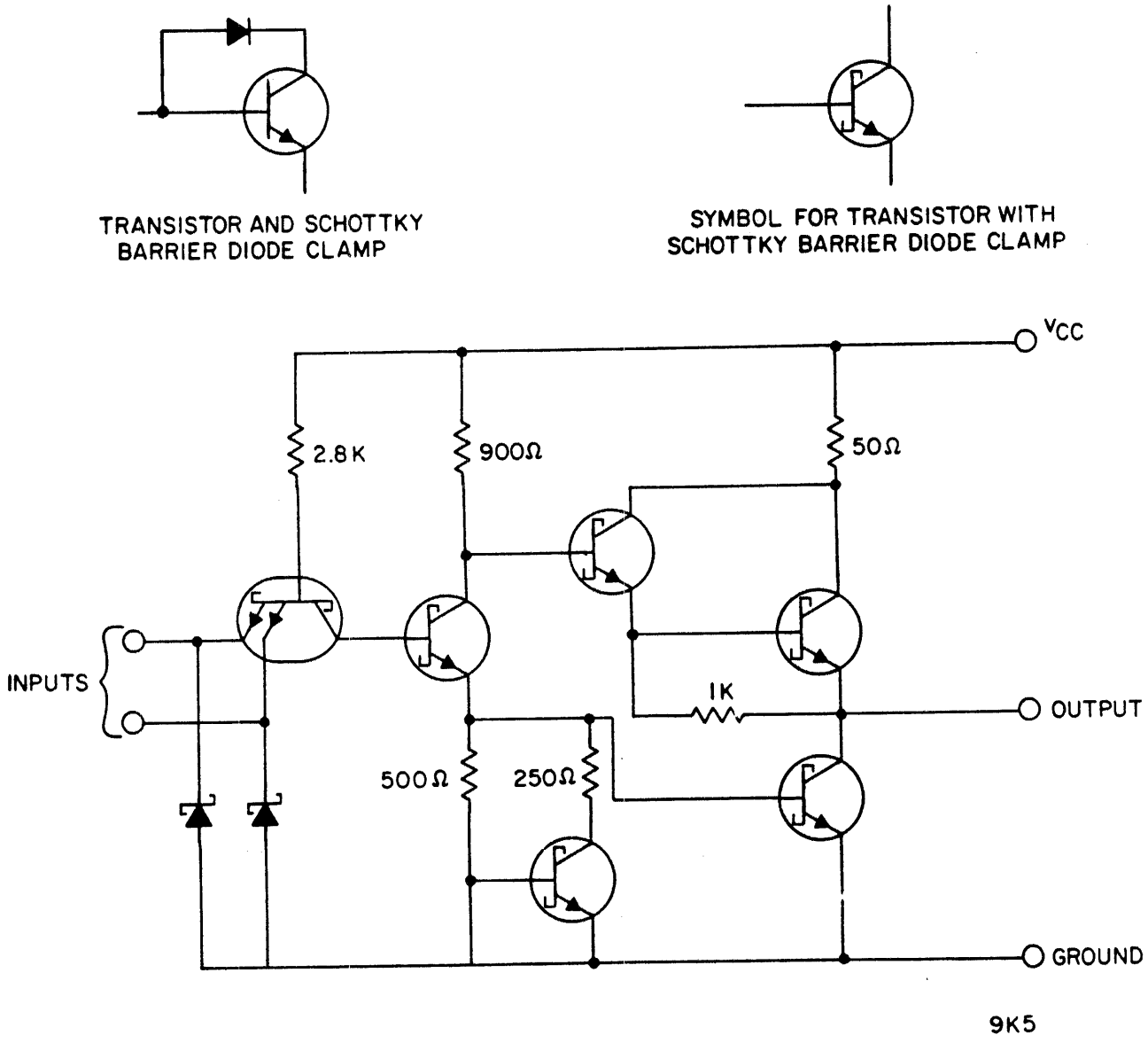


Figure 4-5. TTL NAND Circuit Schottky Series

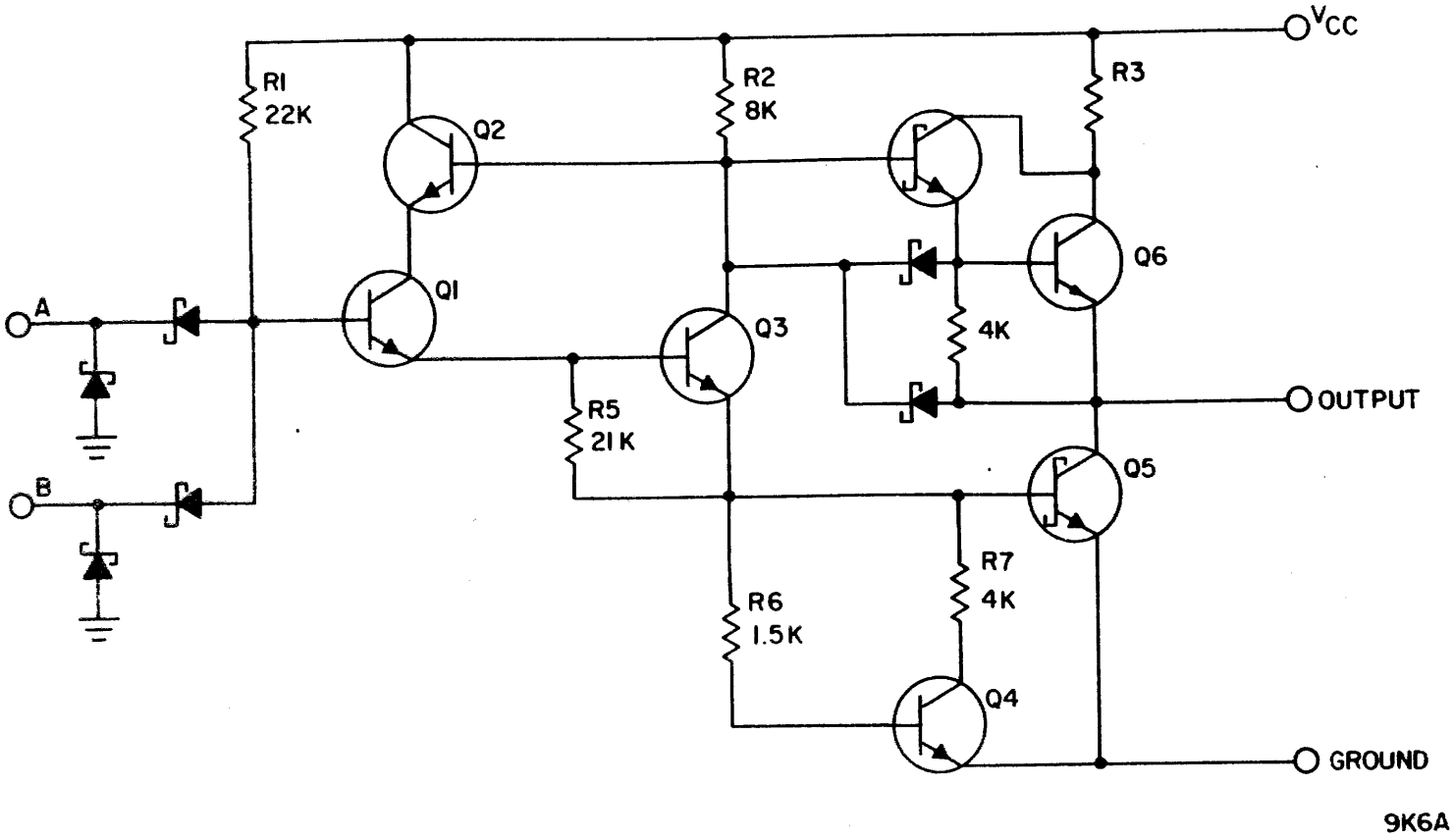


Figure 4-6. TTL NAND Circuit, Low-Power Schottky Series

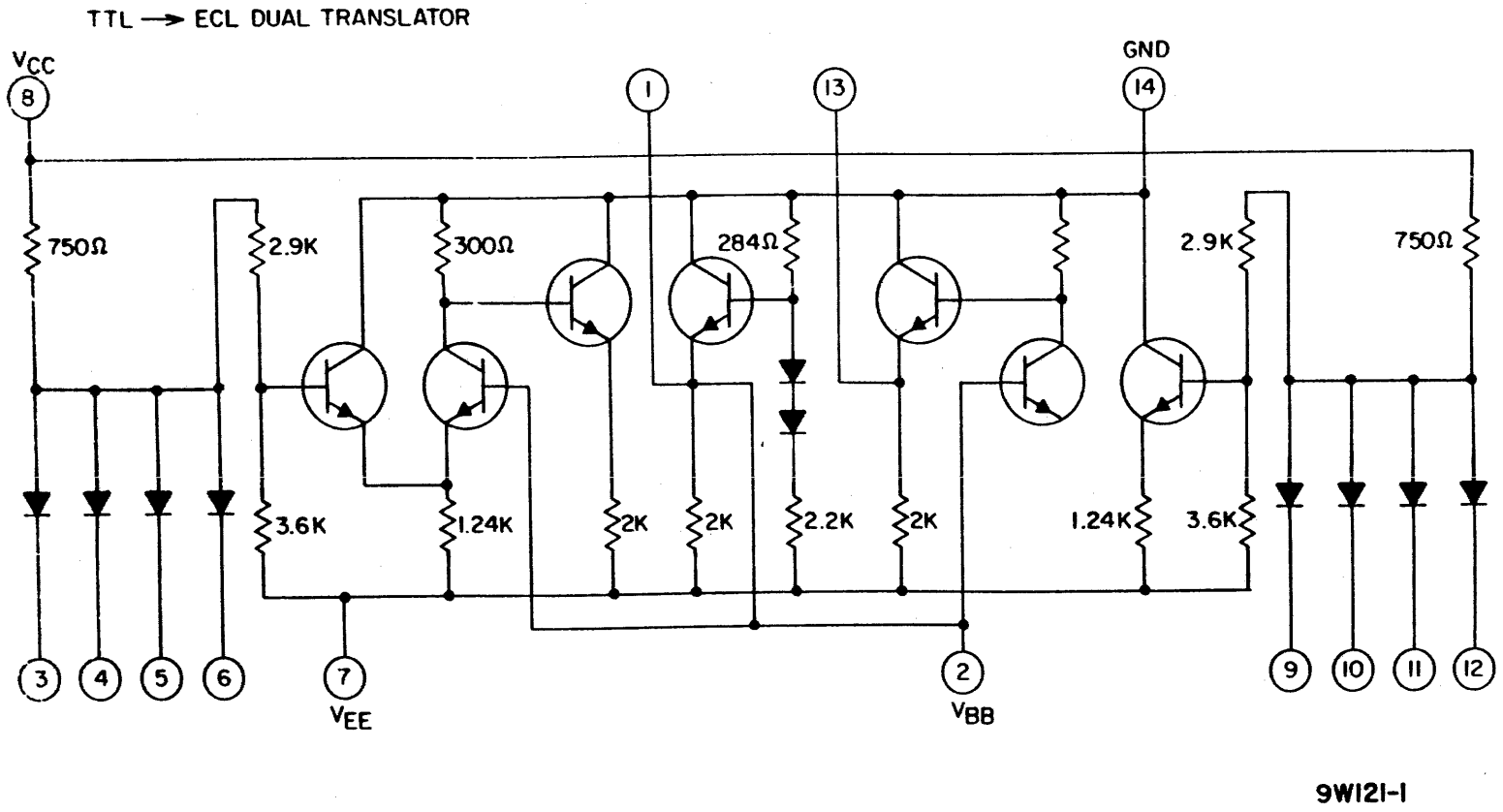


Figure 4-7. TTL/ECL Interface (Sheet 1 of 2)

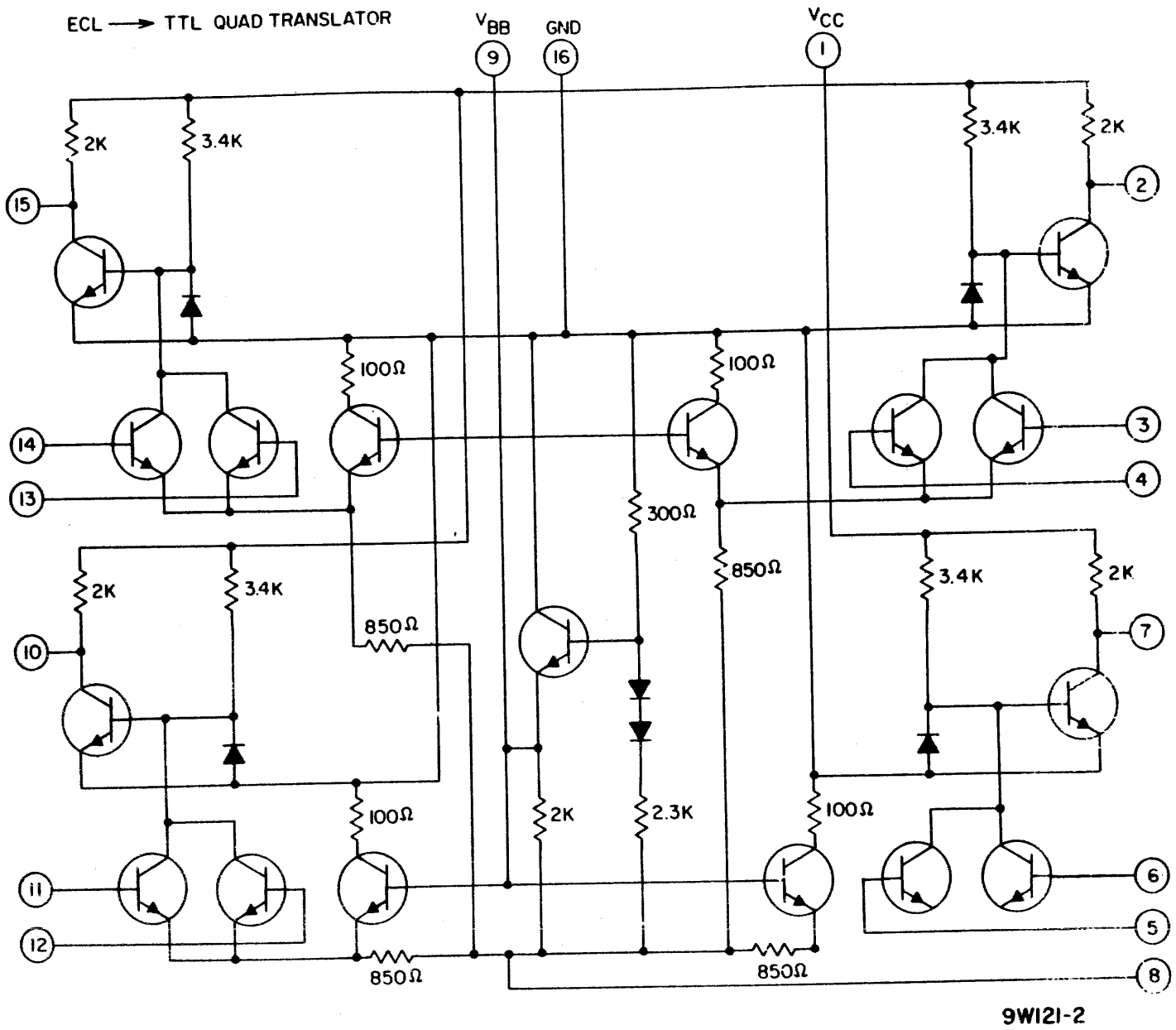


Figure 4-7. TTL/ECL Interface (Sheet 2)

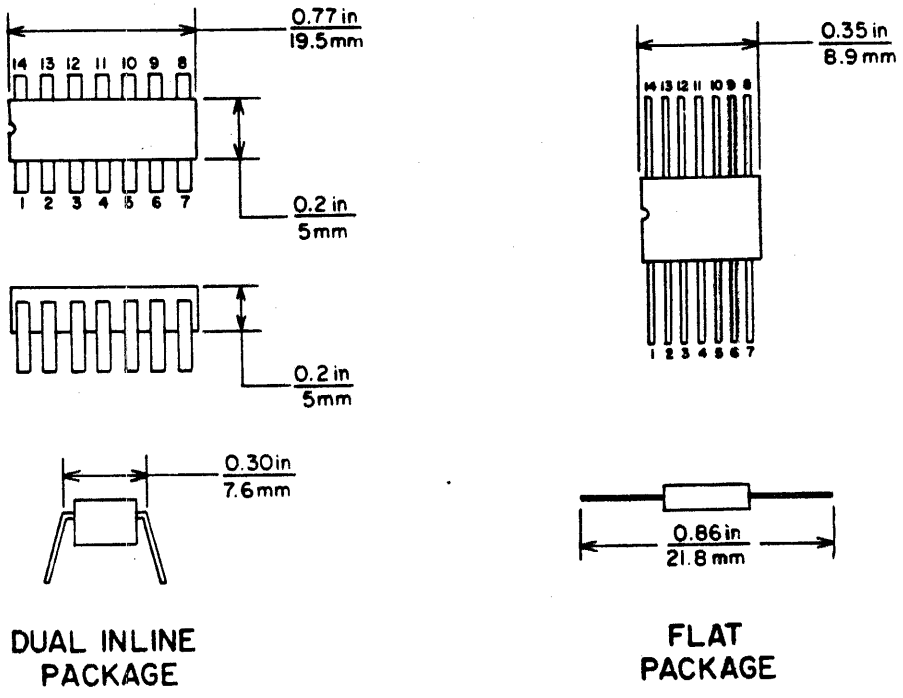


Figure 4-8. Typical TTL Packaging

EMITTER-COUPLED-LOGIC (ECL)

The emitter-coupled-logic (ECL) microcircuit is, by design, nonsaturating, and therefore avoids transistor storage time and its attendant speed limitation, characteristic of transistor-transistor logic (TTL). The high speed of ECL microcircuits has either or both of two characteristics; switching rates of over 50 megahertz and/or gate propagation delays of less than 5 nanoseconds. In general, the gate propagation delays of ECL logic are approximately 2 nanoseconds.

Some of the salient features of ECL microcircuits are as follows:

- High input impedance/low output impedance properties enable large fanout and versatile drive characteristics.
- Minimal power supply noise generation due to differential amplifier design.
- Nearly constant power supply current drain.
- Minimal crosstalk due to low-current switching on signal path.
- Low on-chip power consumption (e.g., less than 8 milliwatts in some complex function chips)
- No line drivers needed due to open emitter outputs of ECL
- Capability of driving twisted pair transmission lines of up to 1000 feet in length.
- Simultaneous complementary outputs available at logic element output without using external inverters.

Logic and Power Levels

	Nom	Min	Max
Supply voltage (V_{EE})	-5.2		
Noise immunity	*	*	*
High output voltage	-0.924	-0.96	-0.81
Low output voltage	-1.75	-1.65	-1.85
High input voltage		-1.105	
Low input voltage		-1.85	-1.475

*Noise immunity of a system involves line impedances, circuit output impedances, propagation delays, and noise margin specifications. Noise margin is a dc parameter calculated from specified points tabulated on an ECL data sheet for the particular microcircuit in question.

CIRCUIT THEORY

A typical ECL gate circuit is shown in figure 4-9 and consists of a differential amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower buffering transistors for transmission line driving. To explain operation of the gate, each of the major sections is discussed in the following paragraphs.

The differential amplifier is an emitter-coupled current switch consisting of transistors Q1 through Q5. The multiple gate inputs provide an OR function (Q1 through Q4) which is amplified by current switch Q5. To understand the gate's operation, assume that all gate inputs are low (-1.75 V and Q1 through Q4 therefore cutoff). Under this condition, Q5 is forward biased, the base being held at -1.29 volts by the bias supply voltage (V_{BB}), and its emitter is at one diode voltage drop (0.8 V) more negative than its base (-2.09 volts total). The base-to-emitter differential then becomes the difference between the low logic level (-1.75 V) and V_{BB} (-1.29 V), or 0.34 volt. Since this voltage is less than the threshold voltage to turn Q1 through Q4 on, they remain in the cutoff state. The current through Q5 will be about 4 milliamperes with a voltage of -2.09 volts at the emitter nodes of Q1 through Q4 using an emitter resistor R_E of about 780 ohms.

The emitter-follower outputs buffer the current switch from loading and restore output voltages to proper ECL levels. The OR output is obtained through Q8 producing the low-level logic signal of -1.75 volts. Similarly, the NOR output is obtained through Q7 producing the high-level logic signal of -0.924 volt.

When any or all of the logic inputs is switched to the high logic level, the appropriate input transistor turns on, a current flows through resistor RC1 in the differential amplifier, and transistor Q5 cannot sustain conduction due to forward biasing, so is cut off. After translating through the emitter followers, the NOR output is a nominal -1.75 volts and the OR output a nominal -0.924 volt.

The differential action of the switching transistors (one section off when the other is on) produces simultaneous complementary signals at the output.

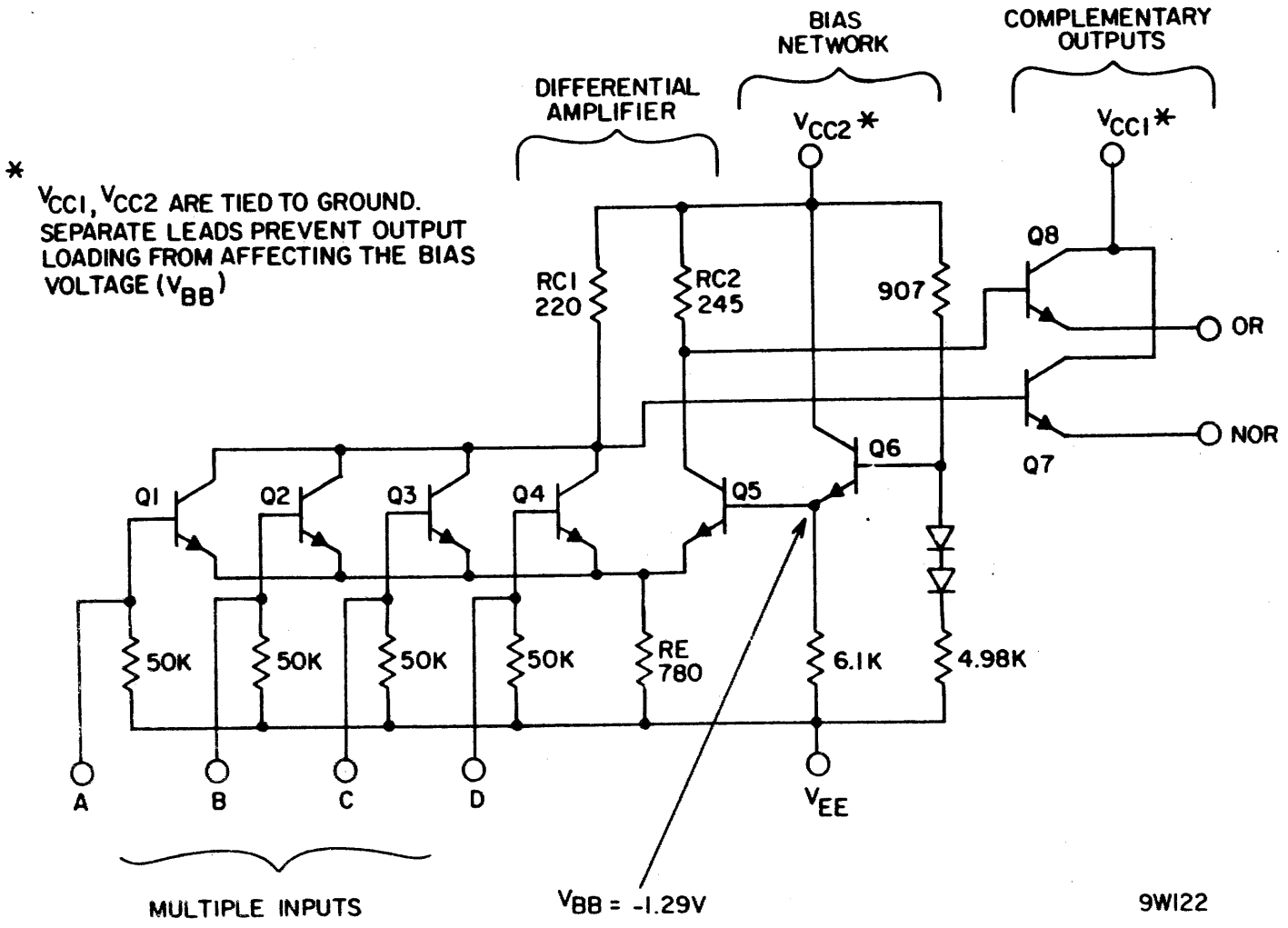


Figure 4-9. Typical ECL Gate

The bias network provides a reference voltage (V_{BB}) of -1.29 volts. This network compensates for variations in power supply voltage and temperature changes to ensure that the bias voltage threshold point remains in the proper operating region.

LOADING CHARACTERISTICS

The differential input to ECL circuits offers several advantages. Its common mode rejection feature offers immunity against power supply noise, and its relatively high input impedance enables any circuit to drive a large number of gate inputs without deterioration of noise margins. The dc loading factor (the number of gate inputs of the same family that can be driven by a circuit output) for ECL circuits is 90. While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit, and therefore affects circuit speed. For ECL circuits, best performance at fanouts of greater than 10 will occur with the use of transmission lines. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance (Z_O) of the transmission line itself are affected by the distributed capacitance and loading due to stubs off the line. Maximum allowable stub lengths for loading of an ECL transmission line vary with line impedance. For example, a transmission line with a Z_O of the line is changed to 100 ohms, stubs may be only 2.8 inches (71.1 mm) long.

The input loading capacitance of an ECL 10109 is 2.9 picofarads. Therefore, fanouts in a non-transmission line environment should be limited to a maximum of 10 loads due to line delay increases which in turn limit speed.

UNUSED INPUTS

The input impedance of the differential amplifier used in the typical ECL circuit is high when the applied signal level is low. Under low signal conditions, any leakage to the input capacitance of the gate may cause a gradual buildup of voltage on the input lead, thereby adversely affecting switching characteristics at low repetition rates. All but a few of the ECL circuits contain input pull-down resistors between the input transistor bases and the -5.2 volt power supply (V_{EE}). Therefore, unused inputs may be left unconnected because leakage current is dissipated by the resistor, keeping inputs sufficiently negative so that circuits will not trigger due to noise coupled into those inputs.

Input pull-down resistors must not be used as pull-down resistors for preceding open-emitter outputs. If an ECL circuit (such as the 10116) does not contain input pull-down resistors, one input of a circuit must be connected to the reference bias supply voltage (V_{BB}) and the other input to V_{EE}.

WIRED LOGIC

Wired-OR gates can be produced in ECL microcircuits by wiring output emitters together (to maximum of 10) outside their respective packages. Wired-OR gates can be connected directly to a bus, also. Propagation delay is increased by approximately 50 picoseconds per wired-OR gate. To economize on power dissipation, a single output pull-down resistor is used per wired-OR gate. Normally, wired-OR gates are connected between gates on the same logic board.

ECL PACKAGING

ECL microcircuits are manufactured in a variety of physical configurations. Two of the more common ones used for the ECL microcircuits described in this manual are the ceramic dual in-line and the plastic dual in-line cases having both 16 and 24 pins, depending upon the size of the package. Figure 4-10 illustrates these packages.

COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR (CMOS)

CMOS microcircuits use four-terminal, enhancement-type field effect transistors (FETs), the symbol for which is given in figure 4-11, to form the basic inverter.

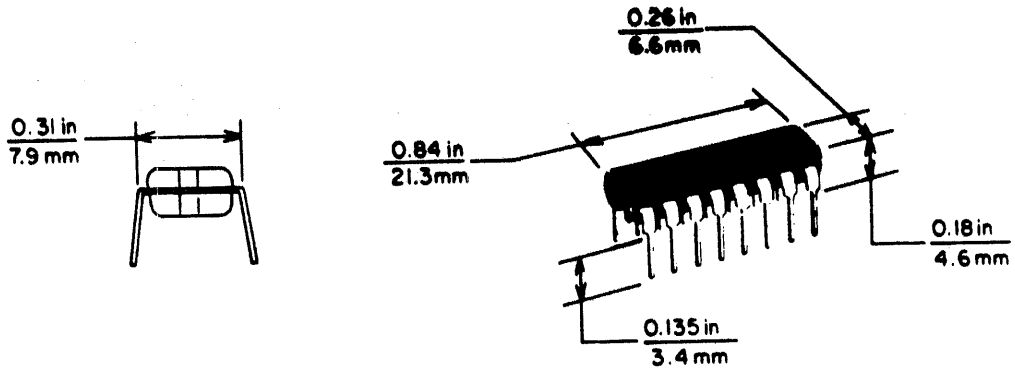
As shown in figure 4-12, a complementary inverter may be formed by applying the input signal to the gates of two opposite-polarity FETs.

In this circuit, a low input signal turns the N-channel transistor Q1 off, and turns the P-channel transistor (Q2) on. The output is shorted to the positive supply, but virtually no load current is drawn if the load is assumed to be another CMOS device with high-impedance input. When the input signal goes high, Q1 is turned on and Q2 is turned on. The output is pulled to ground, but no steady-state current is drawn. Power dissipation in the circuit is thus limited to the crossover points as the device changes state, and with proper design is typically 2 nanowatts per gate.

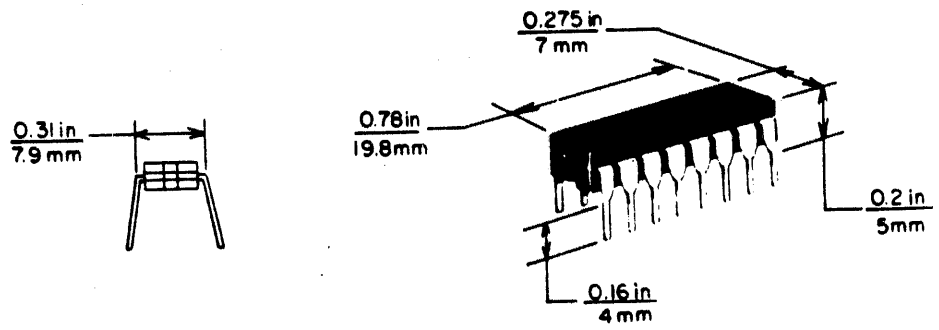
ADVANTAGES/DISADVANTAGES

Advantages

- High circuit density
- High noise immunity
- Lower power dissipation (2.5 nW per gate, typical)
- High fan-out to other CMOS elements (>50)
- Logic swing independent of fanout
- Input threshold is constant over wide temperature range (5% variation, typical)



16-PIN DUAL INLINE PLASTIC (CASE 648)



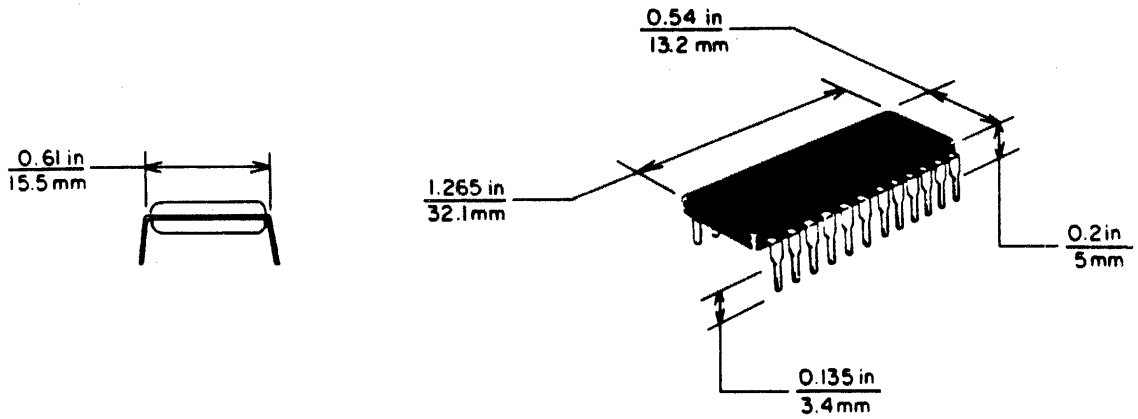
16-PIN DUAL INLINE CERAMIC (CASE 620)

9W123-1

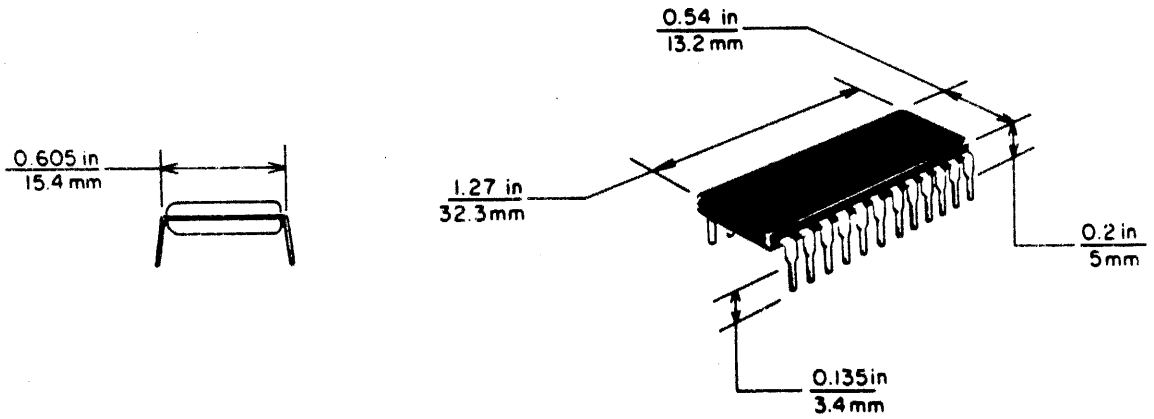
Figure 4-10. Typical TCL Packaging (Sheet 1 of 2)

Disadvantages

- Fabrication complex and more costly than TTL or ECL
- Buffering required when driving several TTL loads
- Level translation required when driving ECL loads
- Characteristic complementary output configuration precludes use of "wired-OR" schemes.
- Inputs extremely electrostatic sensitive -- require special precautions when handling.



24-PIN DUAL INLINE PLASTIC (CASE 649)



24-PIN DUAL INLINE CERAMIC (CASE 623)

9WI23-2

Figure 4-10. Typical ECL Packaging (Sheet 2)

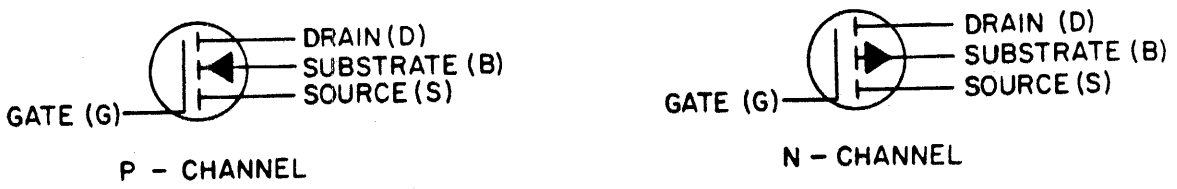


Figure 4-11. FET Symbol

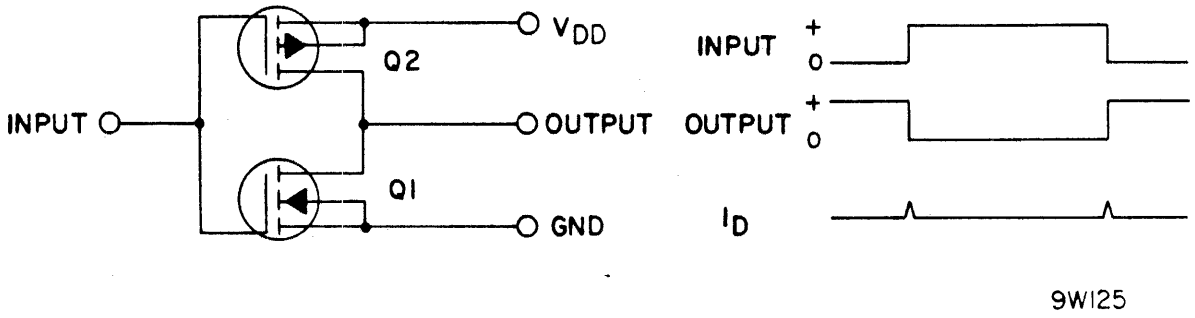


Figure 4-12. Typical CMOS Inverter

OPERATING VOLTAGES

An additional advantage of the CMOS family is its wide range of operation voltage (V_{DD}), which may vary from 3 V dc to 16 V dc although, as is shown later, operating speed suffers for the lower supply voltages. Noise immunity is typically 45% of the supply voltage. The range of input and output voltages is shown below for a Vcc of +5 V.

	Min	Nom	Max
High output voltage	4.99	5.0	-
Low output voltage	-	0	0.01
High input voltage	3.5	5.0	-
Low input voltage	-	0	1.5

INPUT PROTECTION NETWORK

CMOS devices can be seriously damaged if subjected to high electrical fields in the gate oxide region. Any potential over about 100 V between the gate and the substrate breaks down the oxide, resulting in permanent damage. The input protection network shown in figure 4-13 protects the CMOS against voltages in the hundreds region, which is normally sufficient for ICs mounted on a circuit card that is already plugged into a logic-chassis connector. When removing, replacing, shipping, or otherwise handling these electrostatic-sensitive cards, special precautions should be observed to prevent static buildup between the handler and the card. These precautions are outlined in the maintenance manual for any equipment using such cards. The CE is strongly advised against attempting to remove and replace CMOS ICs on these cards; adequate measures to avoid harmful electrostatic discharges during such repair procedures are simply not realizable in the field.

The diode-resistor input protection network shown in figure 4-13 is built into every external input lead as part of the fabrication process. The circuit, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and ground, respectively. (The protection network is not usually shown in CMOS electrical schematic diagrams.)

The series isolation resistor, R_S, is typically 1500 ohms. Diodes D1 and D2 clamp the input voltages between Vcc and ground. Diode D3 is a useful parasitic structure resulting from the diffusion fabrication of R_S. The 6 to 7 ns delay of R_S allows excess energy present at the input pin to be diverted through the protective diodes before reaching the sensitive gate dielectric.

Diodes D1 and D2 have a sharp 30-35 volt avalanche breakdown characteristic. Positive (breakdown mode) and negative (forward conduction) over-voltage protection, with respect to ground when V_{DD} is open, is provided by D1.

Diode D2 similarly provides positive (forward conduction) and negative (breakdown mode) protection with respect to V_{DD} when ground is left open. Both diodes limit the applied voltages to well within the critical breakdown potentials of the gate dielectric. The avalanche characteristic of D3 and D4 is typically 120 V.

REPRESENTATIVE CMOS GATES

Figure 4-14 contrasts a 2-input NAND with a 2-input NOR. The dashed-line boxes enclose the output buffer that is usually a part of the gate. Buffering achieves high performance, standardized output drive, highest noise immunity, and decreased sensitivity to output loading.

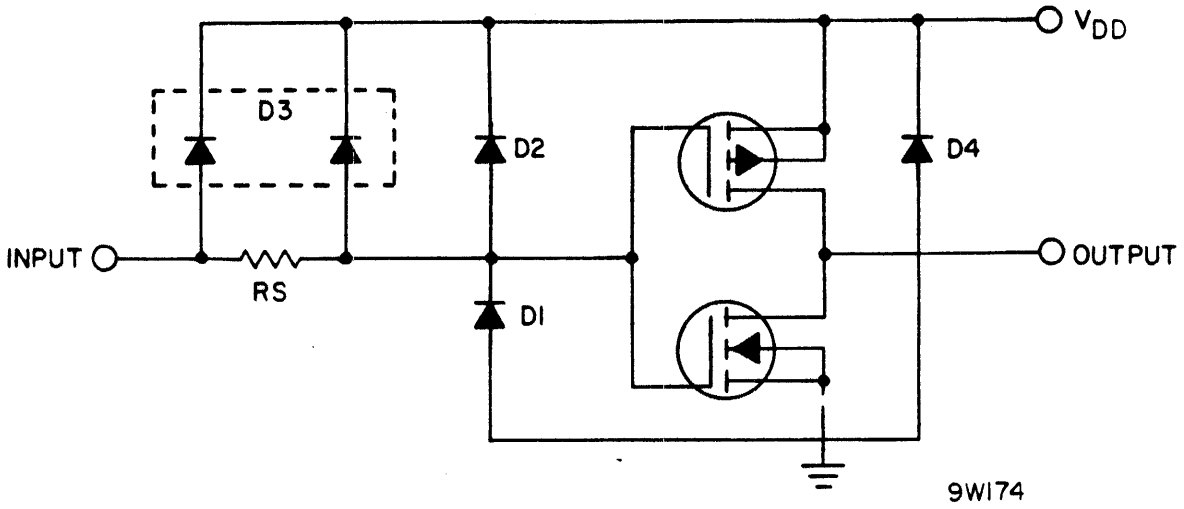
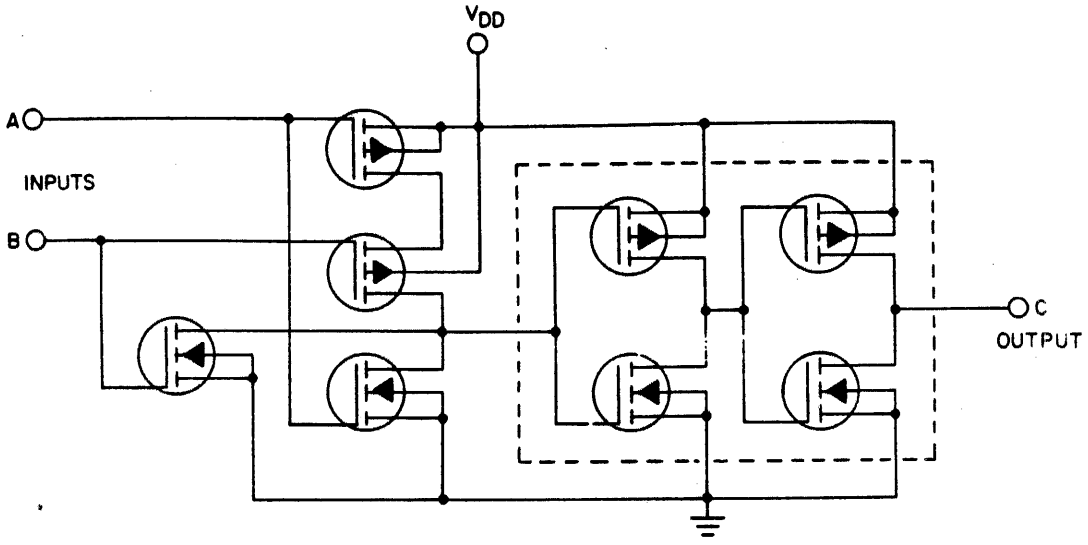


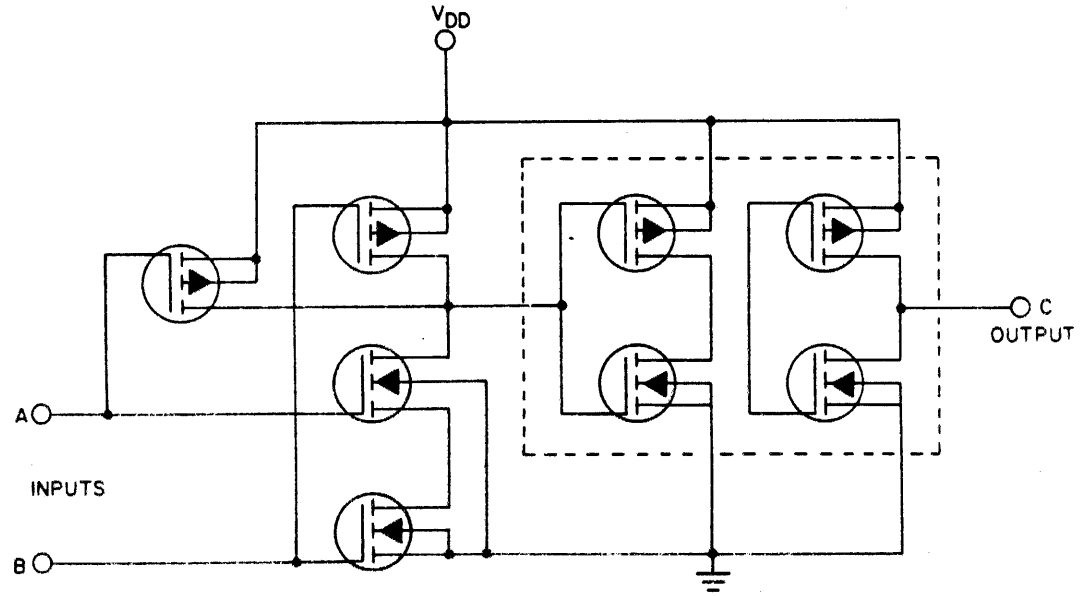
Figure 4-13. Diode-Resistor Input Protection

TRANSMISSION GATE

The transmission gate (TG) is a valuable tool in CMOS design. Two representations of the gate, as found in vendor literature, are shown below. The symbol on the left is used in functional diagrams in this manual.



NOR



NAND

9K14

Figure 4-14. Typical CMOS Gates

The two control inputs, one on the top and the other on the bottom of the symbol, are most usually fed complementary signals. A high on the top control input turns the gate off; a high on the bottom control input turns the gate on.

A typical use of the transmission gate is shown in figure 4-15, which depicts a positive-edge-triggered J-K master-slave FF (circuit 4027). Here, four transmission gates are controlled by complementary clock signals (G, G). When the clock is low, TG1 and TG4 are on, while TG2 and TG3 are off. This logically disconnects the Master from the Slave. Gates 3 and 4, however, are cross-coupled through TG4 (which is on), and the output state remains stable. Assuming that the S and R inputs are inactive, TG1 transmits the state of the J and K inputs to Gates 1 and 2.

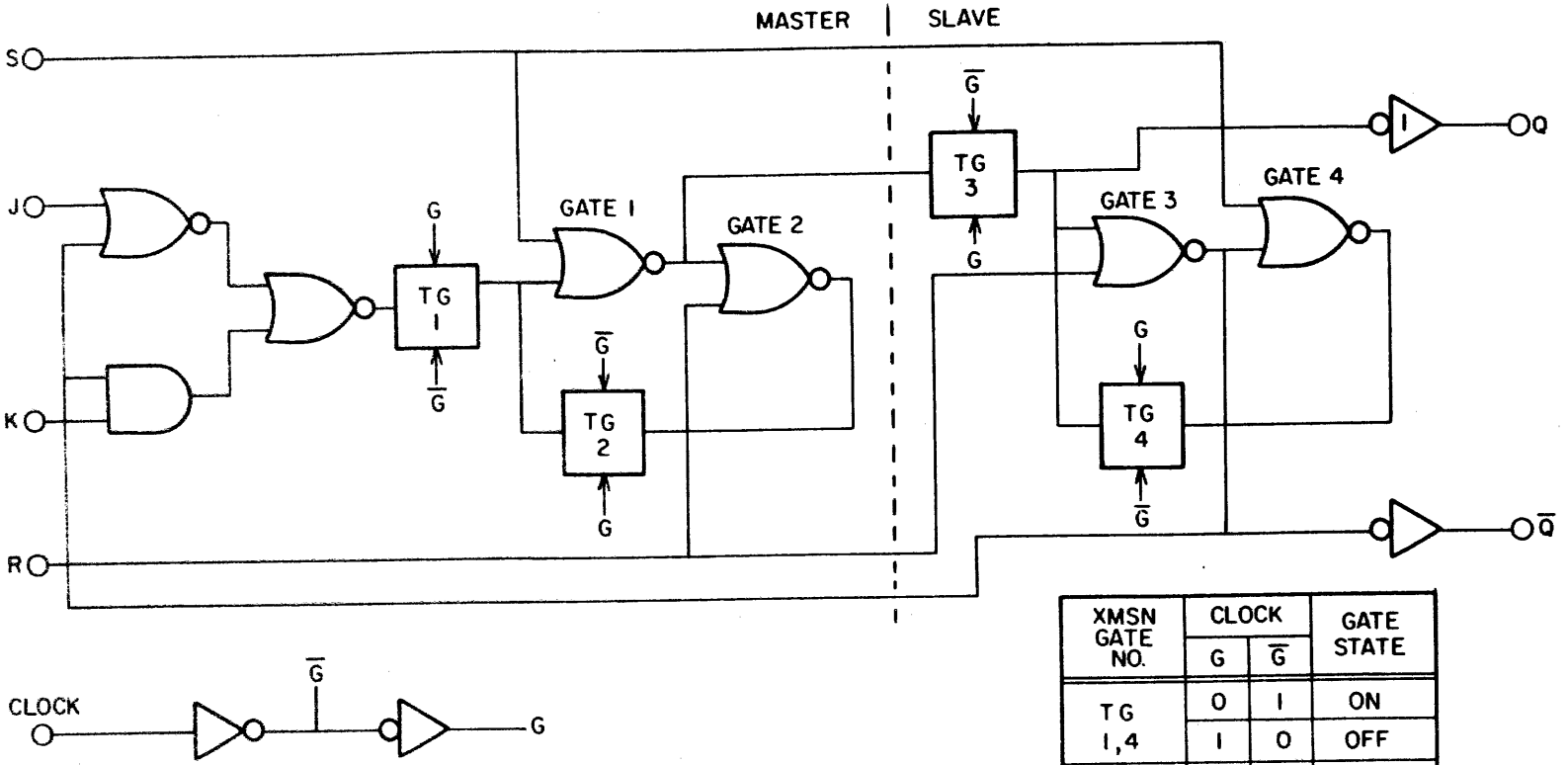
When the clock goes high, TG2 and TG3 turn on, while TG1 and TG4 turn off. Now gates 1 and 2 are cross-coupled through TG2, and latch into the state they held when the low-to-high clock transition took place. With TG3 on, the logic state of the Master section (output of Gate 1) is fed through an inverter to the Q output. Simultaneously, the Q output receives the double inverted output of Gate 1.

OPERATING SPEED

Propagation delay and rise/fall times are functions of the device temperature, operating voltage, and output load capacitance. Delay and transition times increase approximately 1/4 of one percent for each degree Celsius above +25°C, and decrease approximately as the inverse of the operating voltage. For a given V_{DD}, the rise, fall, turn-on and turn-off times are about equal for a load capacitance of 25 picofarads and increase at different rates above that point. The table below gives representative figures.

UNUSED INPUTS

Unused CMOS inputs should be connected to an appropriate logic voltage, depending upon the function of the logic device. Unused NAND inputs should be connected to the +5 V bus, unused NOR inputs to ground. This prevents the input protection structure from floating to some undesired voltage level that prevents the device from functioning properly. In addition, "floating" inputs may be subjected to electrostatic potentials that will permanently damage the device.



XMSN GATE NO.	CLOCK G	CLOCK $\overline{G}$	GATE STATE
TG 1,4	0	1	ON
	1	0	OFF
TG 2,3	0	1	OFF
	1	0	ON

Figure 4-15. Use of Transmission Gates in Flip-Flop Circuit

DELAY/TRANSITION TIMES FOR VARIOUS OPERATING VOLTAGES

Time Measured	V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V			Units
	Load Capacitance									
	15	50	100	15	50	100	15	50	100	pF
Turn off/on	60	120	200	20	40	65	10	25	40	ns
Fall	60	130	220	30	60	110	20	40	70	ns
Rise	60	220	*320	30	90	170	20	60	120	ns

CMOS/TTL INTERFACE

The majority of CMOS devices will not sink the 1.6 mA required for the logical zero input (+0.4 V) to a TTL device. The sinking capability is usually increased by using a 2- or 4-input NOR gate (CMOS) to drive the TTL input. For multiple TTL inputs, special CMOS buffers are used. Sourcing the µA-range needed for a TTL logical one is no problem for the CMOS device.

When coverting from TTL to CMOS, it is important that the TTL output device does not source other TTL circuits, but only the CMOS input. (Sourcing 400 µA for a TTL logical one drops the TTL output to about 2.4 V, considerably below the 3.5 V CMOS threshold required for a logical one.) Sourcing the 10 pA for a CMOS logical one results in a TTL output of around 3.6 V. This is adequate, but provides little noise margin. For this reason, a 2000-ohm pullup resistor is usually inserted between the TTL output and Vcc.

CMOS/ECL INTERFACE

The -5.2 V typical for an ECL supply is easily handled by a CMOS device. If higher negative voltages are advisable because of required CMOS speed, a diode clamp on each ECL input is required to prevent the input from going below the -5.2 V ECL supply.

Level translation is required when going from ECL to CMOS. The 800-mV output swing of an ECL device is not sufficient to drive a CMOS input, so a pnp transistor is used (figure 4-16). A diode in series with the transistor's emitter provides a reverse bias of about 900 mV, which is beyond the output voltage typical of an ECL logical one (-0.924 V). The transistor switches from about -0.9 V to -5.2 V, which is well within the -1.7 V typical for an ECL logical zero output.

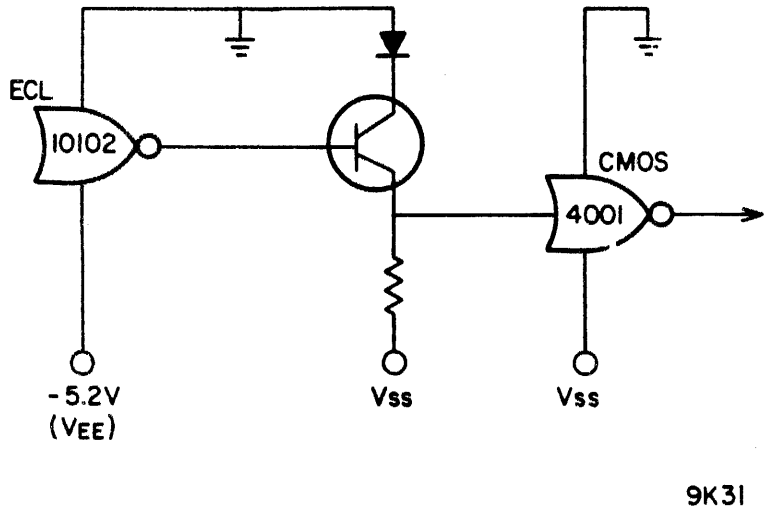


Figure 4-16. ECL-To-CMOS Interface

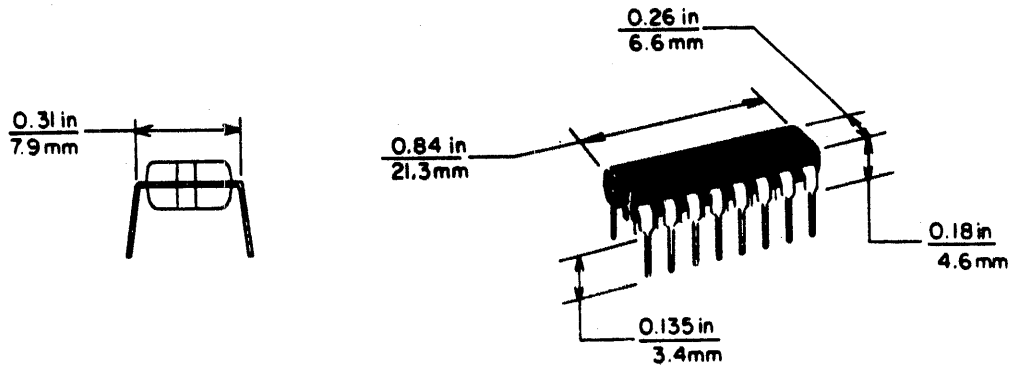
CMOS PACKAGING

CMOS microcircuits are manufactured in dual-inline ceramic (DIC) and dual-inline plastic (DIP) packages with 14, 16, or 24 pins. Figure 4-17 shows the various packaging dimensions.

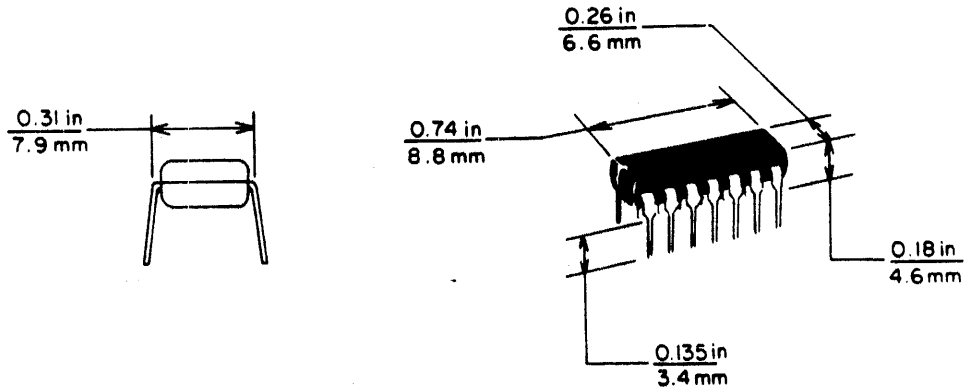
OPERATIONAL AMPLIFIERS

INTRODUCTION

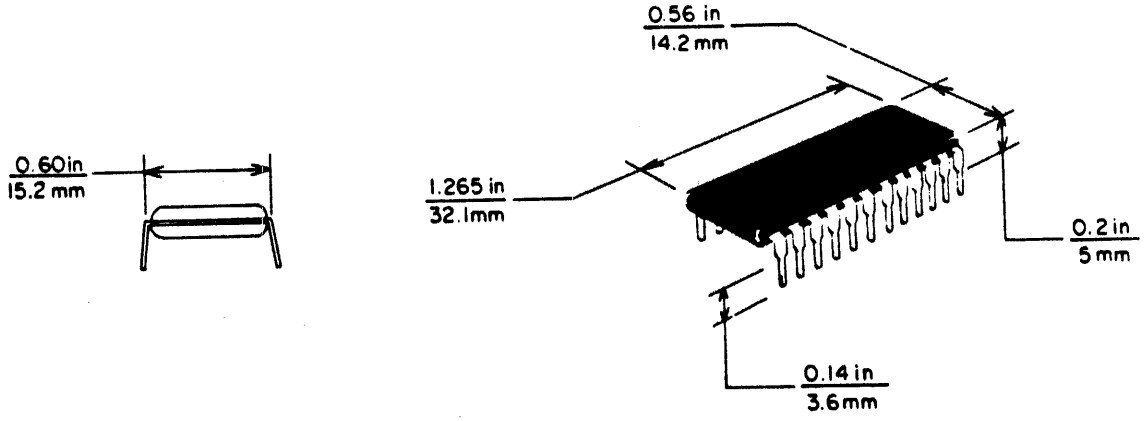
The operational amplifier (op amp) is a high-gain integrated circuit that can apply signals ranging in frequency from dc to its upper frequency limit, which may be more than one megahertz. It is used frequently in a disk drive as a linear amplifier of servo analog signals. Because of its versatility, however, it has multiple applications.



16-PIN DUAL INLINE PLASTIC (DIP) (CASE 648)



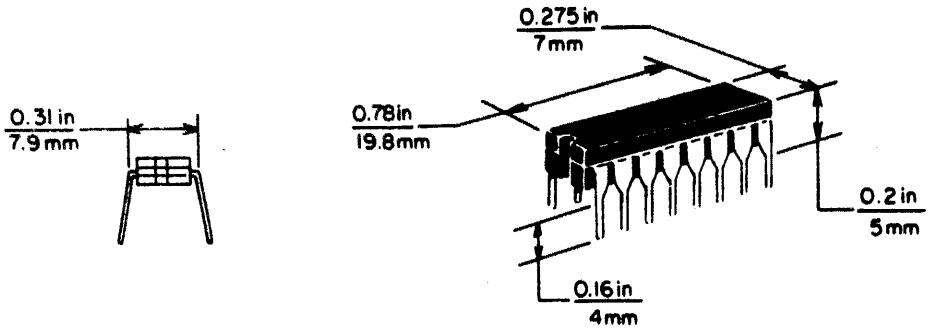
14-PIN DUAL INLINE PLASTIC (DIP) (CASE 646)



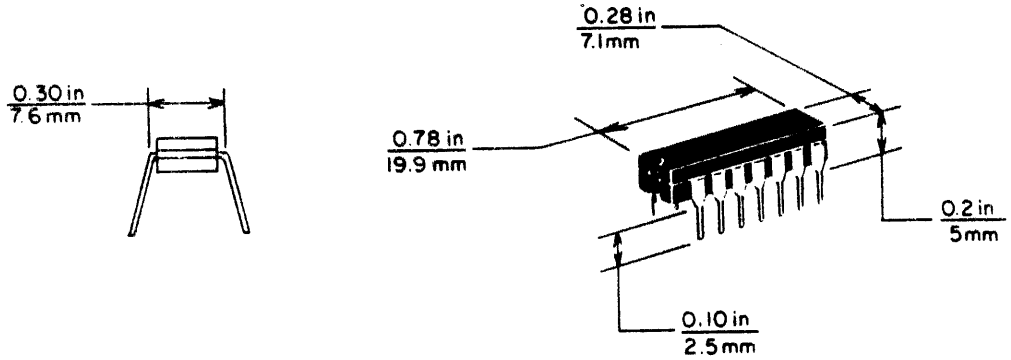
24-PIN DUAL INLINE PLASTIC (DIP) (CASE 709)

9W126-1

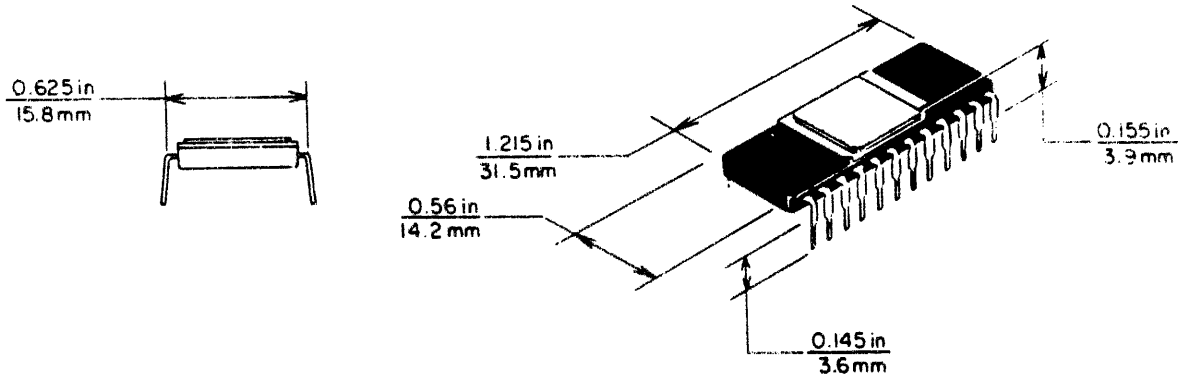
Figure 4-17. Typical CMOS Packaging (Sheet 1 of 2)



16-PIN DUAL INLINE CERAMIC (DIC) (CASE 620)



14-PIN DUAL INLINE CERAMIC (DIC) (CASE 632)



24-PIN DUAL INLINE CERAMIC (DIC) (CASE 684)

9W126-2

Figure 4-17. Typical CMOS Packaging (Sheet 2)

The op amp approaches the following characteristics of an ideal amplifier:

1. Infinite voltage gain
2. Infinite input resistance
3. Zero output resistance
4. Zero offset: output is zero when input is zero
5. High bandwidth frequency response

BASIC CIRCUIT ELEMENTS

Figure 4-18 is a simplified schematic of a typical op amp with its basic feedback network. Detailed circuit analysis information may be obtained by referring to the manuals prepared by the applicable manufacturers.

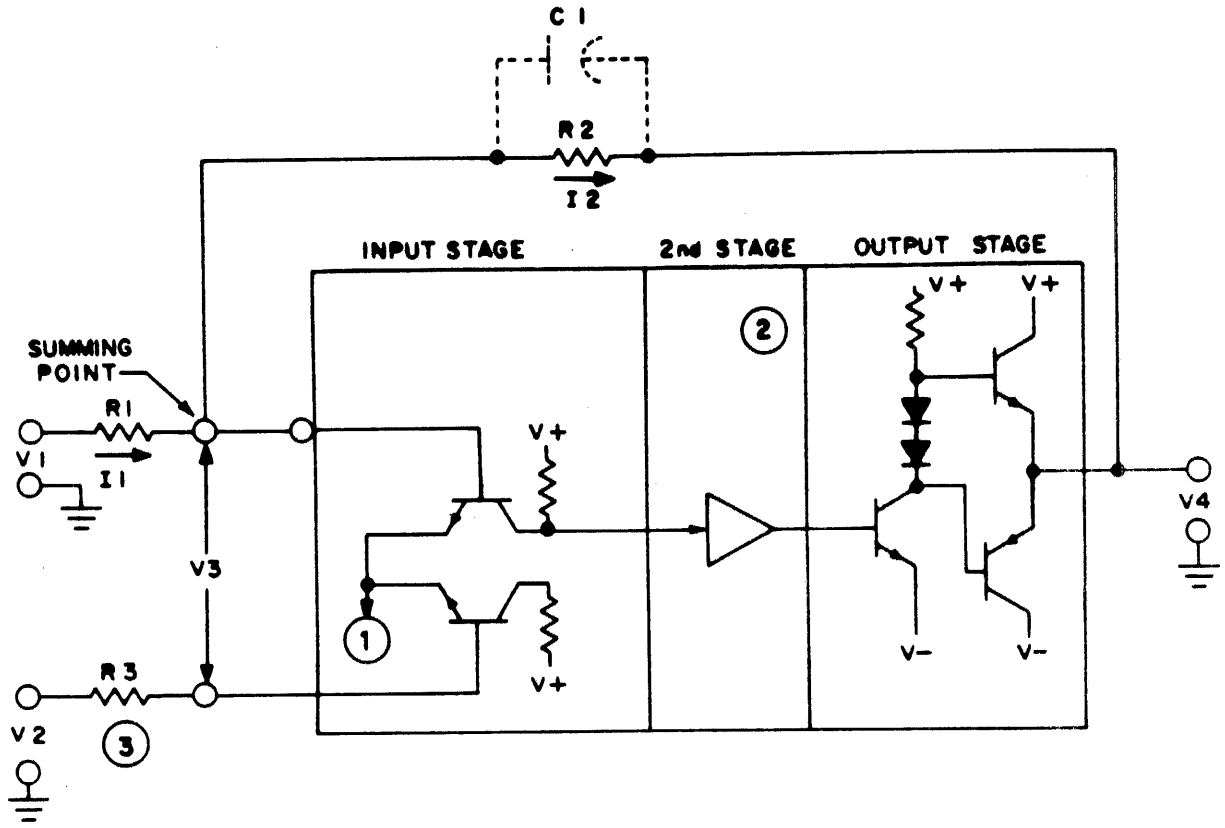
INPUT STAGE

All op amps utilize a differential amplifier in the input stage. This circuit may be relatively simple, as shown, or may consist of multiple circuits with FETs or Darlington-connected transistors. The advantage of this type of amplifier is that it amplifies the difference between the two input signals. For example, if 10 mV are applied to the non-inverting input while 9 mV are applied to the inverting input, the 1 mV difference is amplified. The amplification, which may be a voltage gain of up to 100000, is linear until the op amp saturates or until increasing frequency causes rolloff.

If the same input is applied to both input terminals, the signal is referred to as the common-mode input signal. In the preceding example, 9 mV is the common-mode input, while 1 mV is the differential input. In the ideal op amp, the output is zero with identical inputs; only the difference (1 mV in this case) is amplified. Since the common-mode input is not amplified, signals common to both, such as noise and hum, are cancelled.

SECOND STAGE

Not all op amps have a second stage. If used, however, it may contain additional amplification and level shifting.



NOTES;

1. TO COMMON CONSTANT-CURRENT SOURCE.
2. NOT APPLICABLE TO ALL TYPES. REFER TO MANUFACTURER'S DATA SHEET.
3. FOR BALANCED INPUT IMPEDANCE,

$$R3 = \frac{R1\ R2}{R1+R2}$$

9WI73

Figure 4-18. Simplified Op Amp Schematic

Resistors R1 and R2 provide degenerative feedback to control the overall gain of the circuit. As long as the ratio R2/R1 is low compared to the open loop gain at the operating frequency, circuit gain is independent of the characteristics of the specific op amp.

Rapid analysis of this circuit is possible if two basic principles of op amps are assumed:

1. Insignificant current flows into either input terminal; therefore it is assumed to be zero.

2. The differential voltage (V3) is insignificant and therefore is assumed to be zero.

Rule #1 may be presumed since the input impedance is very high. As a result, all current (I1) entering the summing point must leave it (I2). These currents are:

$$I1 = V1/R1$$

$$I1 = -V4/R2$$

The minus (-V4) indicates that the output is the inversion of the input. Since no current flows into the op amp, I1 must be equal to I2. By Ohm's Law:

$$V4/V1 = -R2/R1 \text{ or } V4 = -V1\ (R2/R1)$$

Therefore, the output is simply the ratio of R2/R1. This linear output/input relationship holds true as long as the input (V1) is not of sufficient amplitude to saturate the op amp.

Resistor R2 is frequently shunted by a capacitor. This controls the roll-off characteristics of the circuit where the full op amp bandwidth is not required. The effective feedback to the input is the resistance of R2 in parallel with the capacitive reactance of C1. Capacitive reactance decreases as frequency increases, the effective impedance of R2/C1 decreases to reduce overall gain.

If C1 is large enough, its charging time becomes more of a factor. The output cannot react as fast as the input may change. This is the integrating or low pass function. For example, doubling the frequency halves the gain. The output is the mathematical integral of the input when the effects of C1 predominate over the effects of R2. Thus, if the input voltage is proportional to velocity, the output is proportional to distance.

Since there is actually a slight current (measured in nanoamperes) entering the differential stage, the difference or unbalance between the two input currents would be amplified. This results in an error known as dc offset; that is, the output would be non-zero with a zero common-mode input. If, however, the currents are made equal, that is, the same input impedance is presented to both, they are therefore common-mode and are cancelled. Resistor R3 is selected to balance out the offset voltage and current by making the impedance to ground of the two inputs equal.

Rule 2 holds true as long as feedback is provided by R2 or its equivalent. As long as the amplifier is not saturated, it will adjust its output voltage to maintain the differential voltage V3 at zero. Therefore, the summing point is at V2. Since V2 is usually at ground potential, the summing point is also at ground. This is a virtual ground; that is, it is at ground potential even though there is no connection between this point and true ground. If the summing point is monitored with an oscilloscope, little or no signal can be observed.

Typical op amp circuit functions are illustrated in figure 4-19.

SCHMITT TRIGGER CIRCUITS

Operational amplifiers can also be connected in the Schmitt trigger configuration (figure 4-20). Note that the degenerative feedback path is not provided. It is replaced by a regenerative feedback path. This is the open-loop configuration: if the voltage at the non-inverting input is greater than the voltage at the inverting input, the output is saturated at its most positive value. Reversing the inputs causes the circuit to slew (change) at its maximum possible rate to saturate negatively.

All Schmitt triggers have hysteresis. Hysteresis is supplied by regenerative feedback from the output to the non-inverting input.

Consider A376 of figure 4-20. Assume the voltage at A is zero. A voltage divider network (not shown) sets point B at +1.28 V). The differential voltage is then zero, so the output starts to switch to a zero-volt output. However, there is now a path from Y to B; the B input becomes less positive than the A input. The output very quickly saturates negatively.

With about -14 V available at Y, the voltage at B is reduced to +1.10 V. The input must now swing to less than +1.10 V for the output to change its state back to positive saturation.

The remaining circuits work in a similar manner.

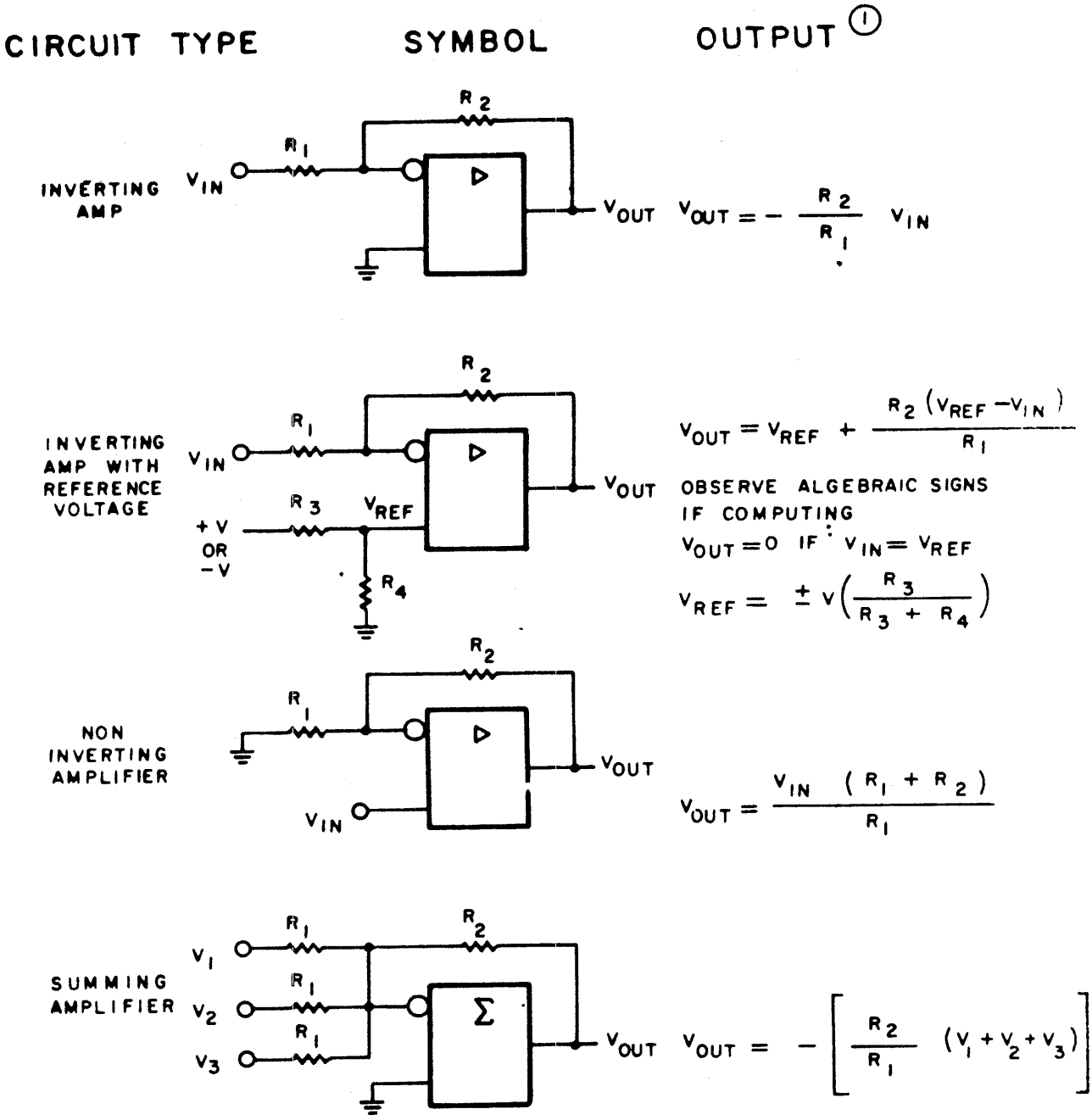
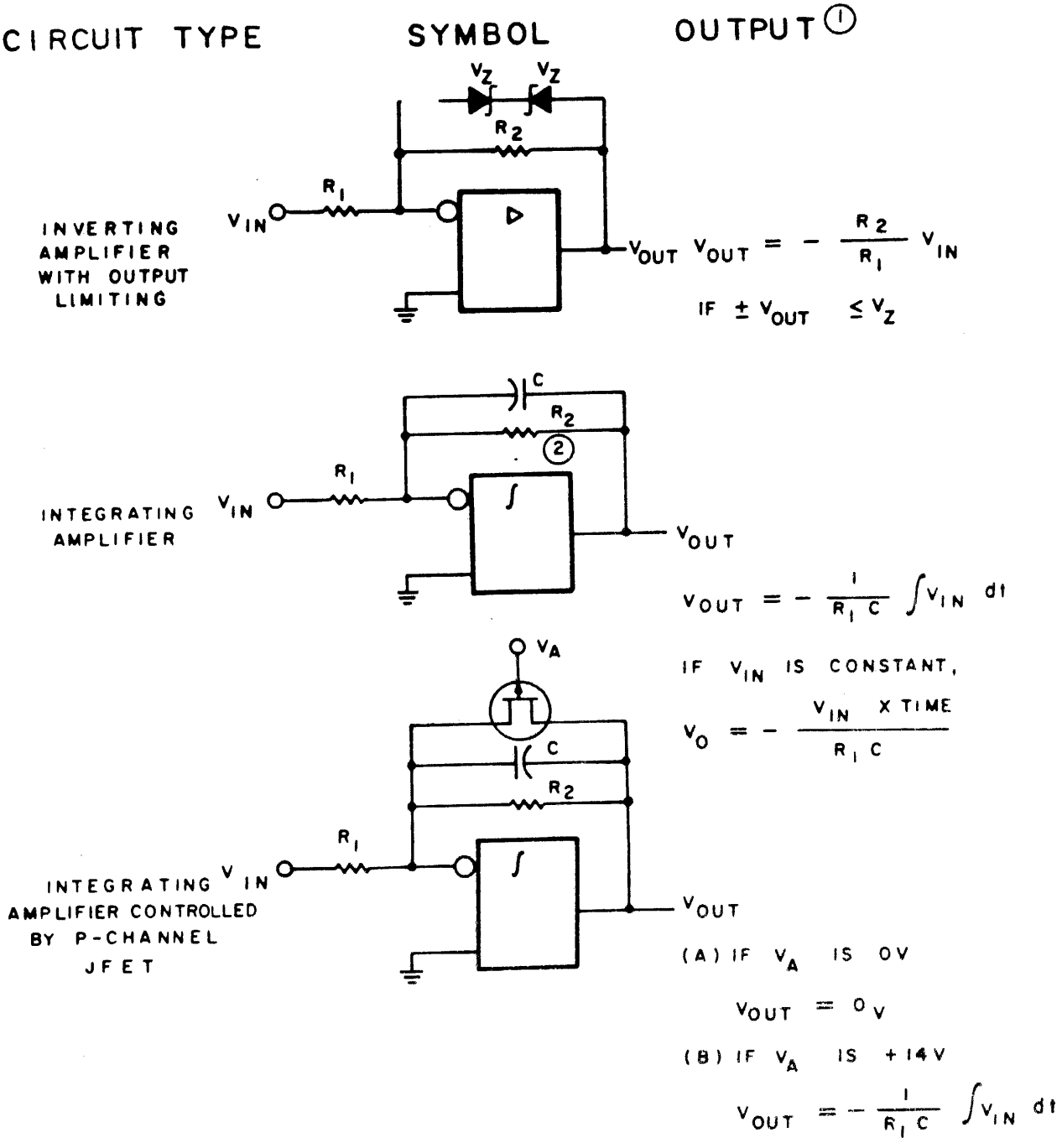


Figure 4-19. Op Amp Circuit Functions (Sheet 1 of 4)



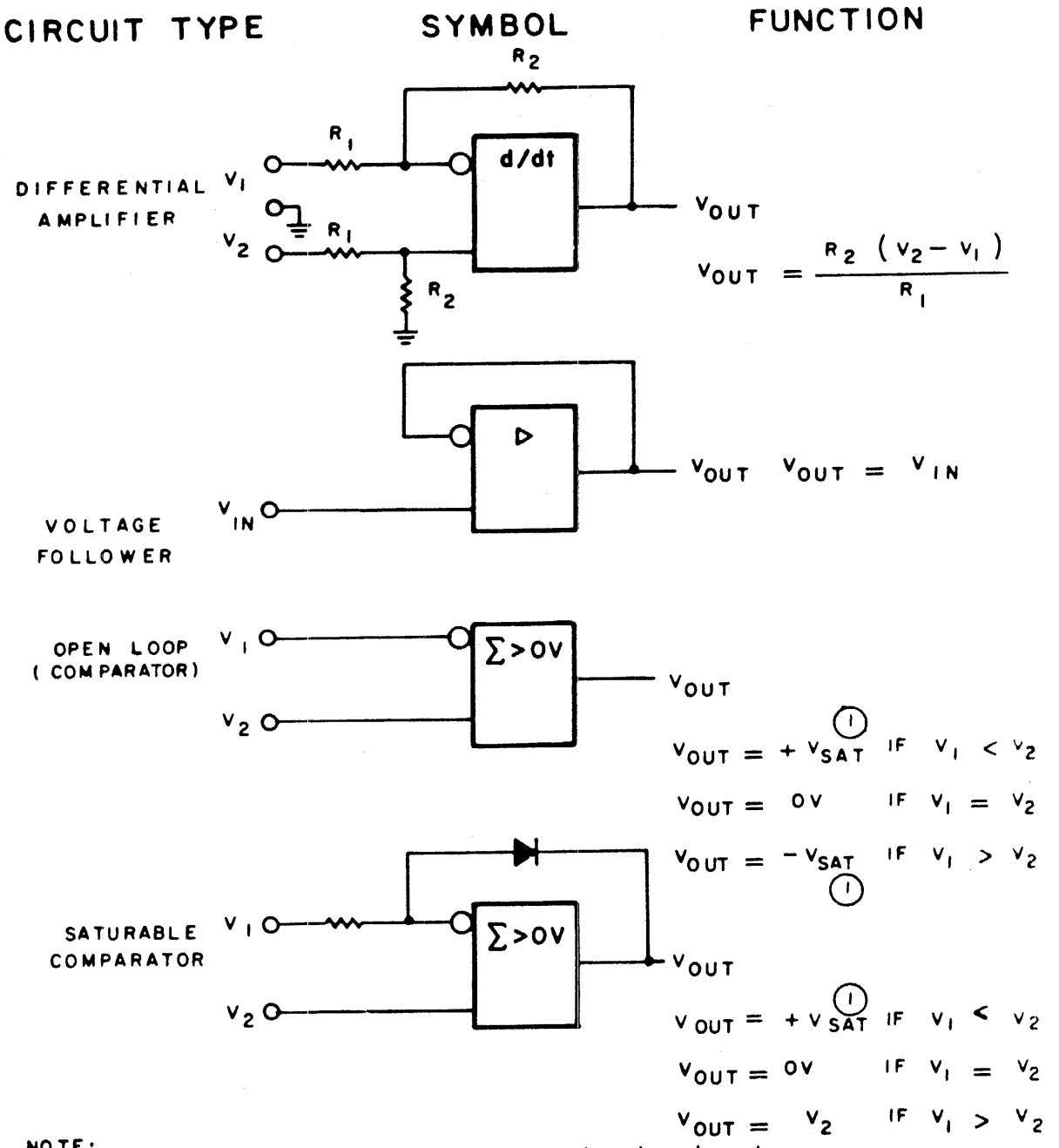
NOTES.

① MINUS SIGN (−) INDICATES THAT OUTPUT IS INVERTED.

② R_2 USED TO PROVIDE DC FEEDBACK TO KEEP OUTPUT SYMMETRICAL ABOUT GROUND.

9W127-2

Figure 4-19. Op Amp Circuit Functions (Sheet 2)



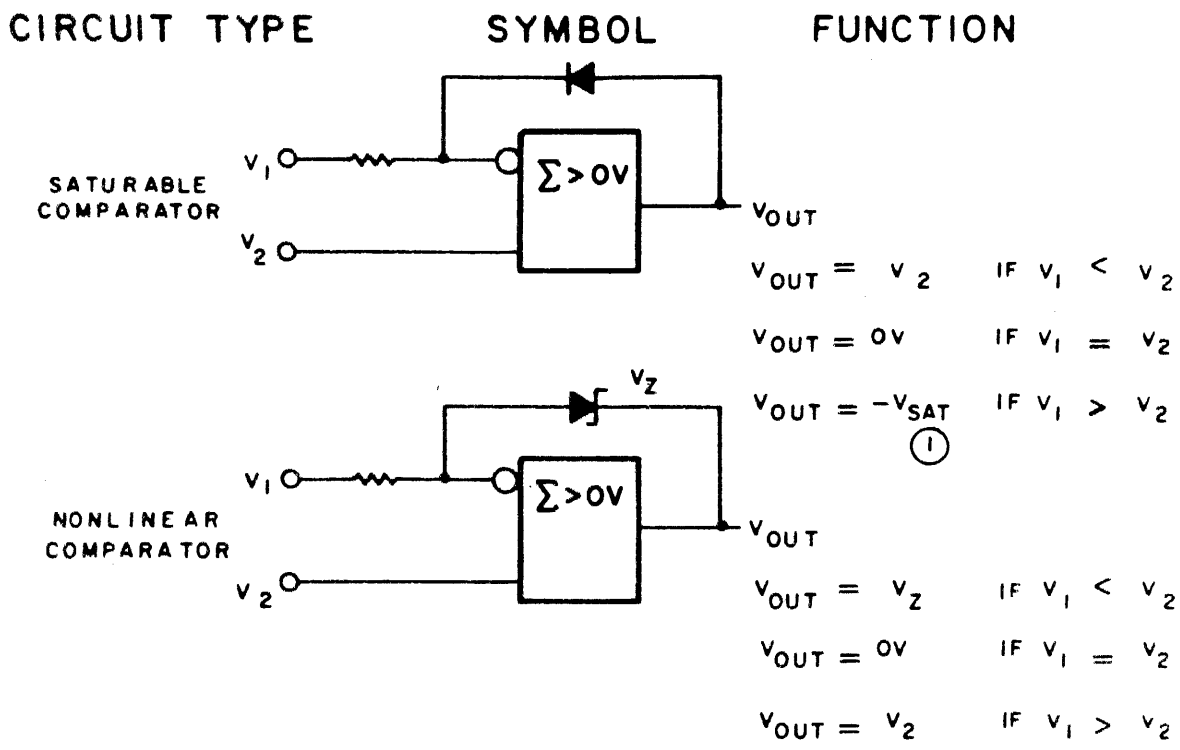
NOTE:

(1) V_{OUT} IS ACTUALLY PRODUCT OF $|V_1| - |V_2|$ X AMPLIFIER OPEN LOOP VOLTAGE GAIN (A_V). $A_V \approx 10{,}000$. V_{OUT} CANNOT ACTUALLY EXCEED THE SATURATION VOLTAGE (V_{SAT}), WHICH IS ABOUT 2 VOLTS LESS THAN THE SUPPLY VOLTAGE.

(2) R_2 USED TO PROVIDE DC FEEDBACK TO KEEP OUTPUT SYMMETRICAL ABOUT GROUND.

9W127-3

Figure 4-19. Op Amp Circuit Functions (Sheet 3)



NOTE:

(1) V_{OUT} IS ACTUALLY PRODUCT OF $|V_1| - |V_2|$ X AMPLIFIER OPEN LOOP VOLTAGE GAIN (A_V). $A_V \approx 10{,}000$. V_{OUT} CANNOT ACTUALLY EXCEED THE SATURATION VOLTAGE (V_{SAT}), WHICH IS ABOUT 2 VOLTS LESS THAN THE SUPPLY VOLTAGE.

9W127-4

Figure 4-19. Op Amp Circuit Functions (Sheet 4)

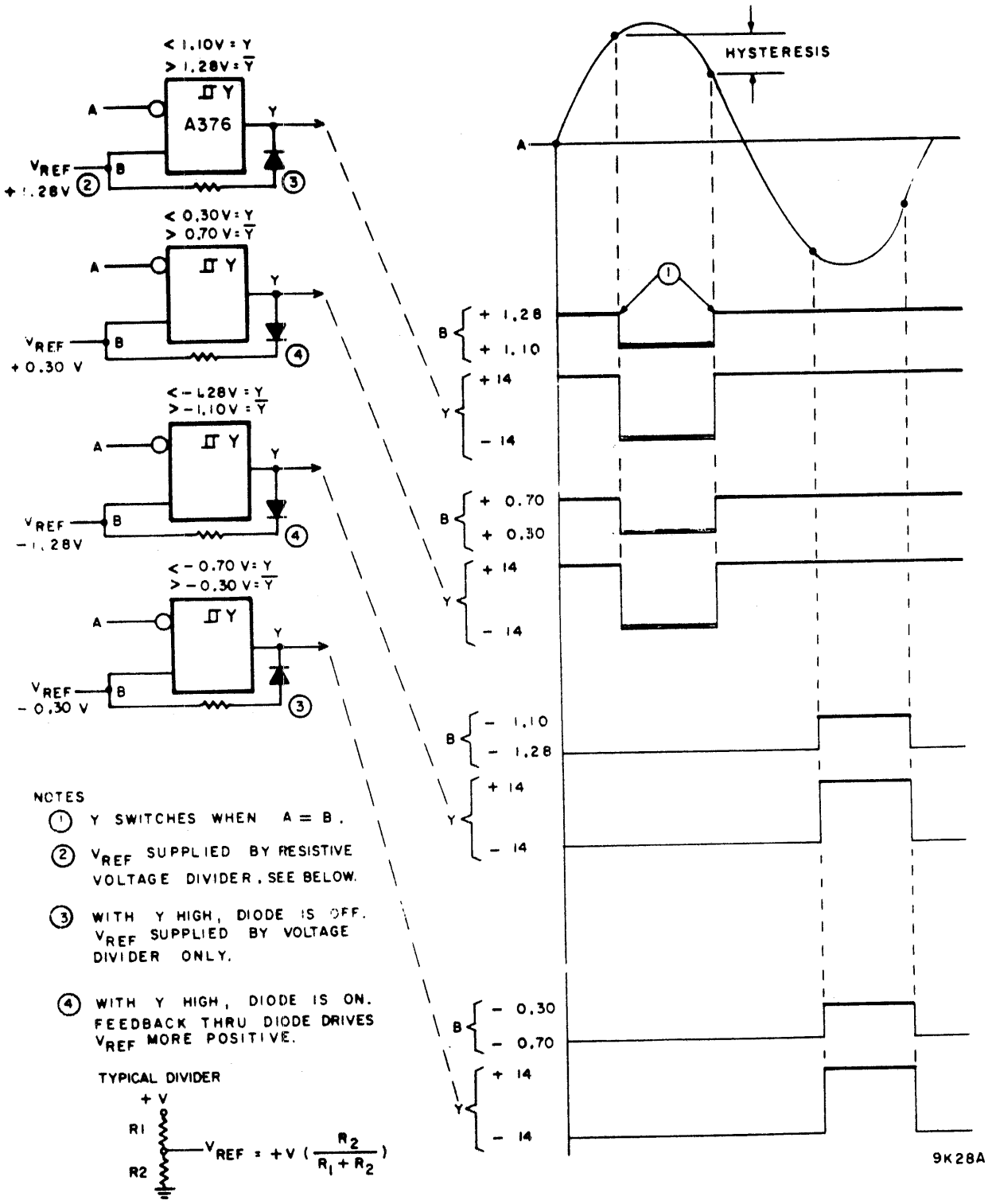


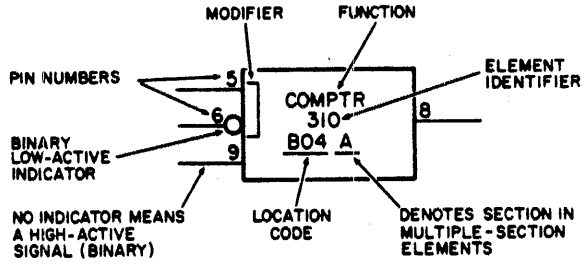
Figure 4-20. Op Amp Used as Schmitt Trigger

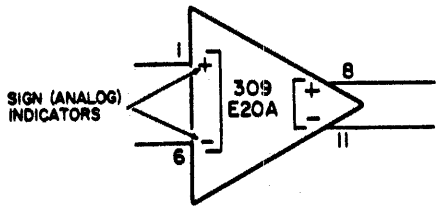
LOGIC SYMBOLOGY

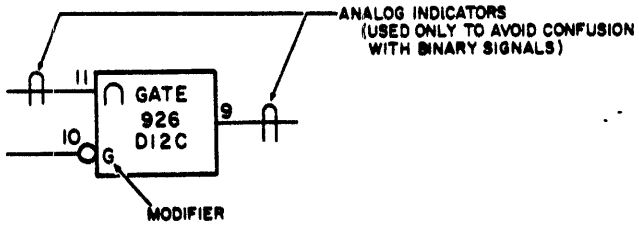
SECTION 4B

GENERAL

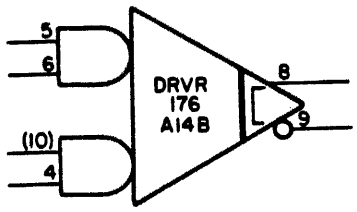
The logic symbols used with the data sheets in section 3 of this manual follow MIL STD 806-B/C. In addition to the symbol outline itself, a symbol consists of a function name, various modifiers and/or indicators, pin numbers, an element identifier, and a location code that specifies the physical placement of the microcircuit on the logic module or printed-circuit board. These items are placed within or adjacent to the symbol outline, as shown below.







The function name is usually omitted from distinctive-shape symbols (see the amplifier above), but may be included to further define the general function implied by the distinctive shape:



The pin number in parentheses (10) denotes a pin that is common to other section(s) of the microcircuit. In this case, the symbol for the "A" section of the driver would show pin 10 without the parentheses.

SUPPLEMENTAL NOTATION

In addition to the standard 806-B/C logic-symbol modifiers -- D, R (CLR), LD, Q, weighting modifiers, etc. -- and which are discussed in the individual microcircuit descriptions, the data sheets in section 4C employ the additional symbol notations reviewed below.

MODIFIERS

G	An enable signal. A viable output from the microcircuit depends upon the presence (active state) of the G modifier. Hence, G is often referred to as a dependency modifier.
⊐,⊏	A differential input, or a differential output, respectively. The microcircuit derives the differential by comparing the input signals appearing at the two pins spanned by the bracket, or by applying the generated differential signal to the two bracketed output pins.
▌	The heavy vertical bar is a mnemonic device to aid in distinguishing line drivers and receivers from other microcircuits using the same distinctive-shape (amplifier) symbol. The bar always appears within the symbol (as do all modifiers). It is near the input (left) side of the symbol for receivers and near the output side (right) for drivers.

INDICATORS

Except for the analog sign indicators shown below, indicators appear in or on the signal lines just outside the logic symbol, but as close to it as practical without interfering with pin numbers.

Non-standard logic level: The slash on an input or output line identifies a binary level that differs from that considered standard. (Refer to standard levels for TTL, ECL, CMOS as given in section 4A.)

+,−

Analog sign indicators: The plus sign indicates the normal (non-inverting) analog input or output; the minus sign identifies the inverting input or output. Analog signals most frequently appear in pairs. When they do not, only the inverting signal (-) is identified; the lack of a + indicator, then, implies a non-inverting input or output.

Analog signal: The inverted "U" (input or output) on a signal line is used only if confusion between analog and digital signals might otherwise arise. It is not used, for example, in conjunction with the + and - modifiers that in themselves define a signal as analog.

Binary (digital) logic: This symbol differentiates binary from analog signals (input or output). It is used only if confusion might otherwise arise.

Open-collector output: If the open-collector output line is continued on another diagram sheet, the diamond may be repeated just to the left of the off-sheet indication. This serves as a reminder that the pull-up resistor (usually part of a wired-OR configuration for which the diamond is the ANSI representation) is shown elsewhere. (A microcircuit element can only drive an open collector low; the high level must be provided by a source outside the element.)

Dynamic Active State (positive): This represents the transition from the inactive to active static state of the input (not merely the presence of the active static state).

Dynamic Active State (negative): This represents the transition from the active to inactive static state of the input (not merely the presence of the inactive static state).

FUNCTION NAMES

The following list identifies the function names found within the logic symbols on the data sheets of section 4C. Abbreviations are those approved by ANSI Y1.1 (1972). Function names that are not abbreviated within the symbol (e.g., ADDER) have been omitted.

COMPTR	Comparator
CNTR-4	Counter (4-bit)
CUR AMP	Operational Current Amplifier
D/A CONV	Digital-to analog Converter
DCDR	Decoder
DRVR	Driver
E COMPTR	Voltage Comparator
FF	Flip-flop
MUX	Multiplexer
MV	Multivibrator
m VR	Voltage Regulator (The regulated output-voltage value replaces "m".)
OP AMP	Operational Amplifier
RCVR	Receiver
↓SR-4	Shift Register (4-bit). (The arrow direction here indicates a right -- or down -- shift.
SS	Single-shot (also One-shot)
∩ Gate	Analog Gate
∅ f DET	Phase-frequency Detector

INTRODUCTION

This section contains a cream-colored divider sheet separating the information into two subsections:

1. Introductory remarks.

2. Data sheets arranged by element identifier.

In subsection 2, the element identifier also appears as a page number at the bottom of the data sheet. Speed variations (H, L, LS, S, etc.) are shown on the same page as the basic circuit.

DATA SHEET INTERPRETATION

All of the data sheets in this section contain the following kinds of information:

1. LOGIC SYMBOL - The 806-B/C symbol for the high-active version of the microcircuit and, where applicable, the alternate low-active version. Pin numbers are included as part of the symbol. Special notations to clarify the various input and output functions are added when helpful, but are not to be construed as part of the symbol.

2. DESCRIPTION - An explanation of the function or functions performed by the microcircuit.

3. NOTES - Helpful information, such as:

   - Vendor reference number
   - Package pin configuration. Defines pins used for external voltage sources (V_{CC}, V_{EE}, GND, etc.) and keys, slots or marks used to orient the microcircuit.

In addition, the following information is included on individual data sheets, when applicable:

DATA SHEETS

SECTION 4C

4. FUNCTIONAL DIAGRAM - Basic logic symbols (NAND, NOR, FF, etc.) arranged to show the internal logic of the microcircuit.

5. TRUTH TABLE - A table showing the state(s) of the microcircuit's output for varying input conditions.

6. TIMING DIAGRAM - Used to clarify complex timing relationships between inputs and outputs.

DATA SHEET LIST

The list on this page shows the order in which the data sheets appear, and also provides a quick reference to the family (TTL, ECL, CMOS) to which a particular microcircuit belongs. If a circuit requires more than one data sheet, the number of sheets is given in parentheses.

TTL	OP AMPS	TTL	ECL
140	300	500	10102
141	301	501	10104
143	306	519	10105
145	307	520	10106
146	309	521	10116
148	315	527	10125
149	316	538	10131
158	320	581	12040
159	322	916	
161	326	926	
162	327	986	
164	329		
172	330		
173	331		
175	332/353		
176	333		
182	338	CMOS	
188	339	4001	
191		4011	
195		4017	
200		4023	
202		4027	
208		4049	

DESCRIPTION

Element 140 is a 4-section (quad), 2-input, positive NAND gate.

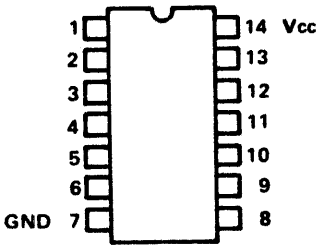
NOTES:

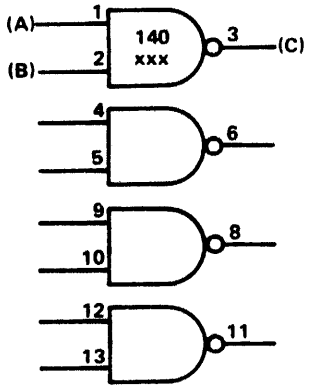
1. Element identifier and location (xxx) repeated for each section.

2. Vendor identification:

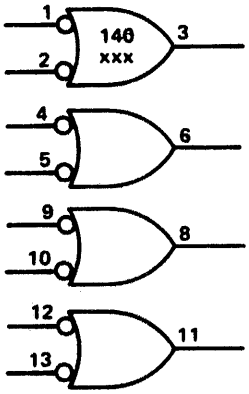
Element	Vendor Number
140	7400, 9002
140H	74H00
140L	74L00
140LS	74LS00
140S	74S00

3. Package pin configuration.





OR



LOGIC SYMBOL

TRUTH TABLE

A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

DESCRIPTION

Element 141 is a 3-section, 3-input, positive NAND gate.

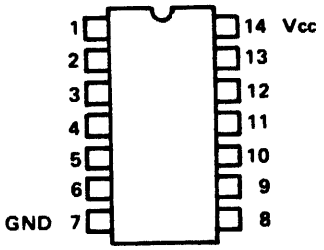
NOTES:

1. Element identifier and location (xxx) repeated for each section.

2. Vendor identification:

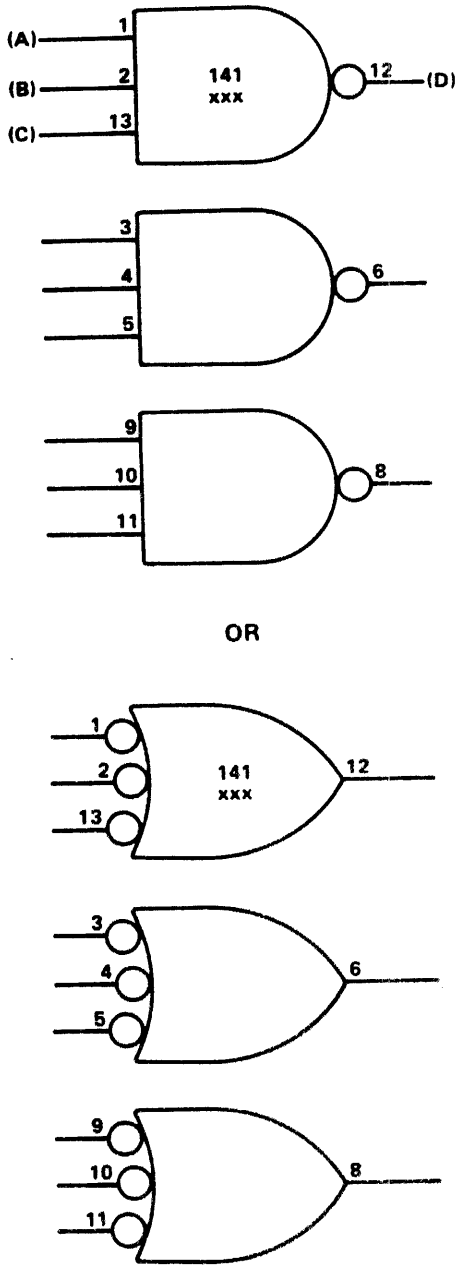
Element	Vendor Number
141	7410, 9003
141H	74H10
141L	74L10
141LS	74LS10
141S	74S10

3. Package pin configuration:



TRUTH TABLE

A	B	C	D
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L



LOGIC SYMBOL

141
Sheet 1 of 1

DESCRIPTION

Element 143 is a 2-section, 4-input, positive NAND gate.

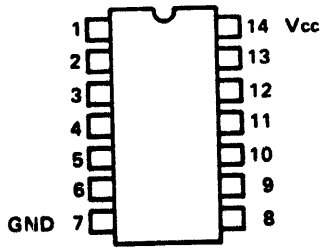
NOTES:

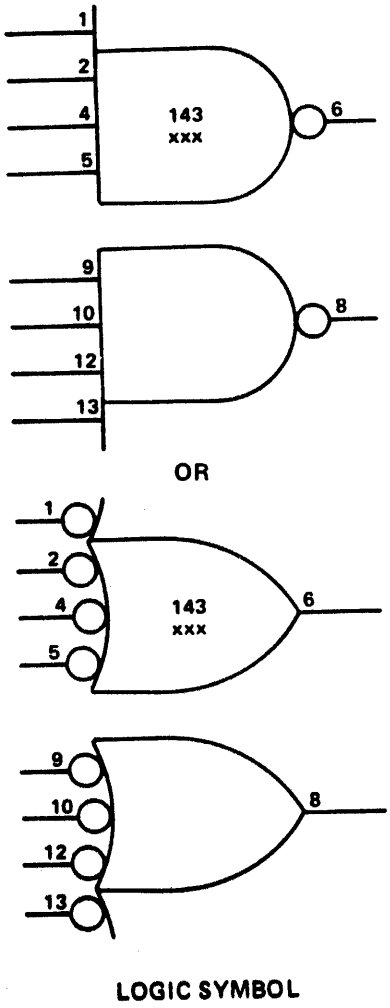
1. Element identifier and location (xxx) repeated for each section.

2. Vendor identification:

Element	Vendor Number
143	7440, 9009
143H	74H40
143S	74S40

3. Package pin configuration.





LOGIC SYMBOL

143
Sheet 1 of 1

DESCRIPTION

Circuit 145 is a dual, expandable AND-OR-INVERT gate. The second section of this circuit is expandable. If not expanded, pins 11 and 12 are open.

NOTES:

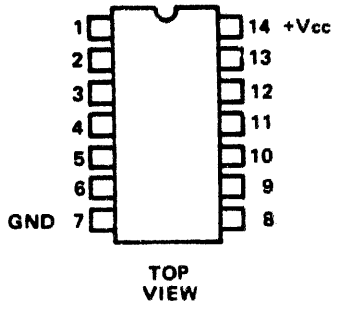
1. Element identifier and location (xxx) repeated for each section.

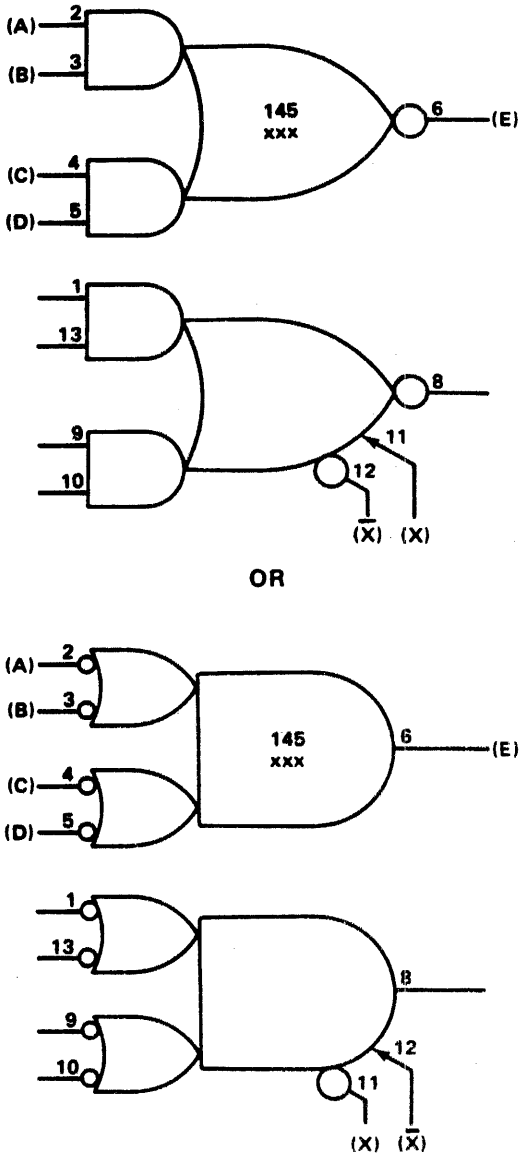
2. If not used, expander pins may not be shown.

3. Vendor identification:

Element	Vendor Number
145	9005
145H	74H50

3. Package pin configuration.





LOGIC SYMBOL

TRUTH TABLE

A	B	C	D	X	$\overline{X}$	E
Y	Y	Y	Y	H	L	L
L	L	L	L	L	H	H
L	L	L	H	L	H	H
L	L	H	L	L	H	H
L	L	H	H	L	H	L
L	H	L	L	L	H	H
L	H	L	H	L	H	H
L	H	H	L	L	H	H
L	H	H	H	L	H	L
H	L	L	L	L	H	H
H	L	L	H	L	H	H
H	L	H	L	L	H	H
H	L	H	H	L	H	L
H	H	L	L	L	H	L
H	H	L	H	L	H	L
H	H	H	L	L	H	L
H	H	H	H	L	H	L

L = LOW; H = HIGH; Y = DON'T CARE.
For non-expandable section, or if expander inputs (X,$\overline{X}$) are not used, disregard shaded portion of Truth Table.

DESCRIPTION

Element 146 is a six-section (hex) inverter.

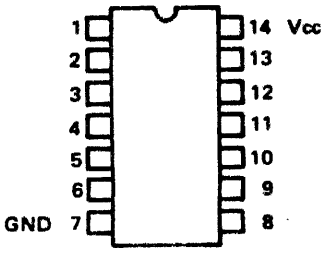
NOTES:

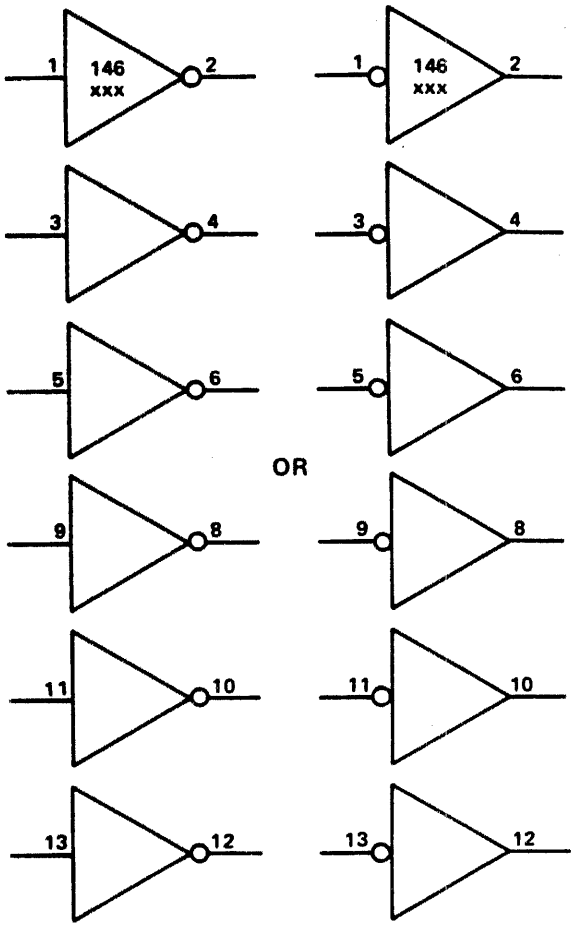
1. Element identifier and location (xxx) repeated for each section.

2. Vendor identification:

Element	Vendor Number
146	7404, 9016
146H	74H04
146L	74L04
146LS	74LS04
146S	74S04

3. Package pin configuration.





LOGIC SYMBOL

146
Sheet 1 of 1

DESCRIPTION

Element 148 is a quad, 2-input, positive NOR gate.

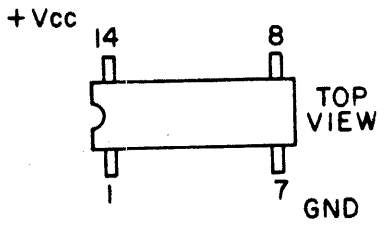
NOTES:

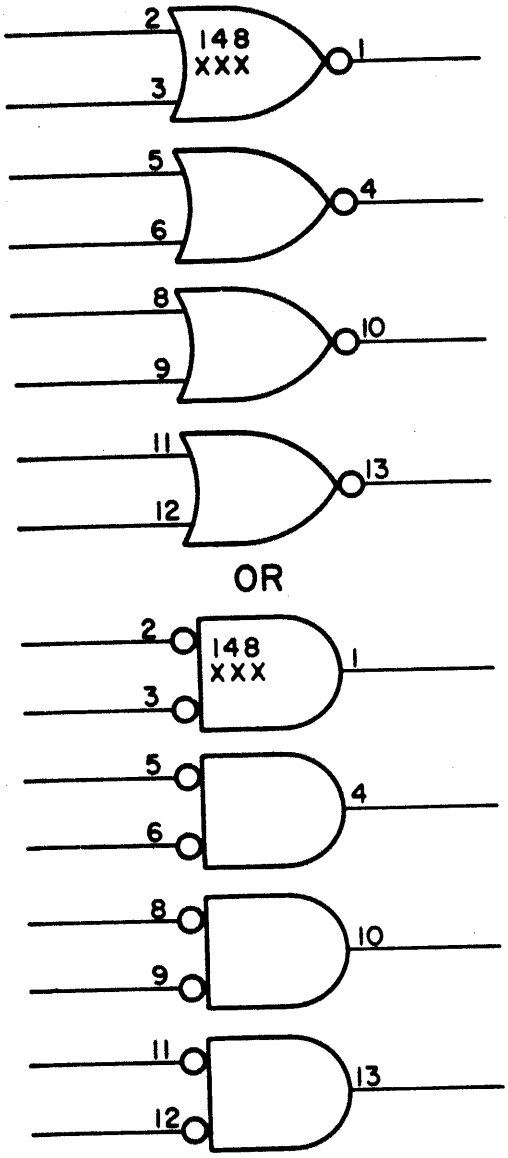
1. Symbols may appear separately.

2. Vendor identification:

Element	Vendor Number
148	7402
148L	74L02
148LS	74LS02
148S	74S02

3. Package pin configuration.





LOGIC SYMBOL

148
Sheet 1 of 1

DESCRIPTION

The 149 circuit is a quad, 2-input, Exclusive OR gate that performs the function $Y = A\bar{B} + \bar{A}B$. When the input states are complementary, the output goes to the high level.

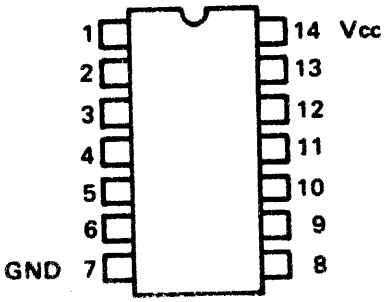
NOTES:

1. Element identifier and location (xxx) repeated for each section.

2. Vendor identification:

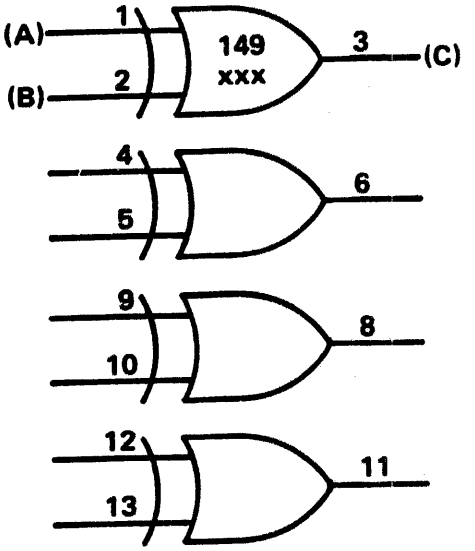
Element	Vendor Number
149	7486
149H	3021
149LS	74LS86
149S	74S86

3. Package pin configuration.

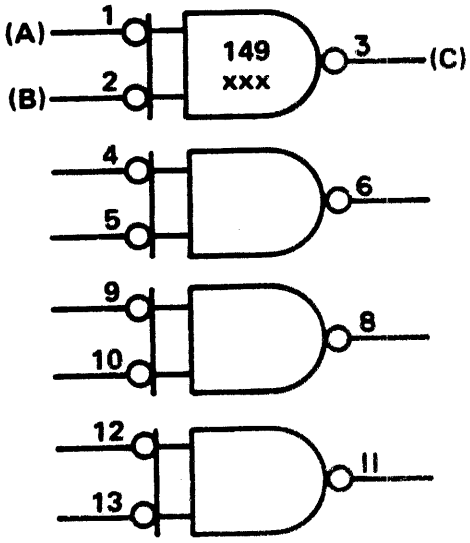


TRUTH TABLE
(ANY SECTION)

A	B	C
L	L	L
L	H	H
H	L	H
H	H	L



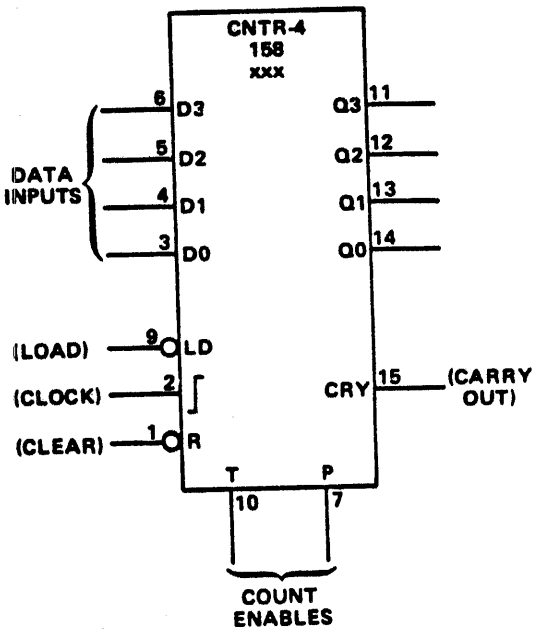
OR



LOGIC SYMBOL

DESCRIPTION

The 158 circuit is a 4-bit synchronous binary counter. This circuit can be preloaded with data at the data inputs when the load input is low. This disables the counter and enables the data inputs. Input data will be transferred to the outputs the next time the clock input has a low to high transition.



In order for the counter to count, the load (pin 9), clear (R), and P and T enable inputs must be high. A low level to the clear input will clear the outputs to low level regardless of the level to any other input.

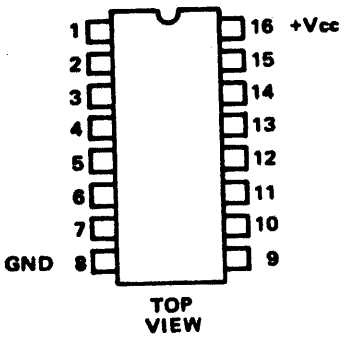
When P is low, the clock input is disabled so that the counter can not count. When T is low, the clock input and carry output are both disabled.

NOTES:

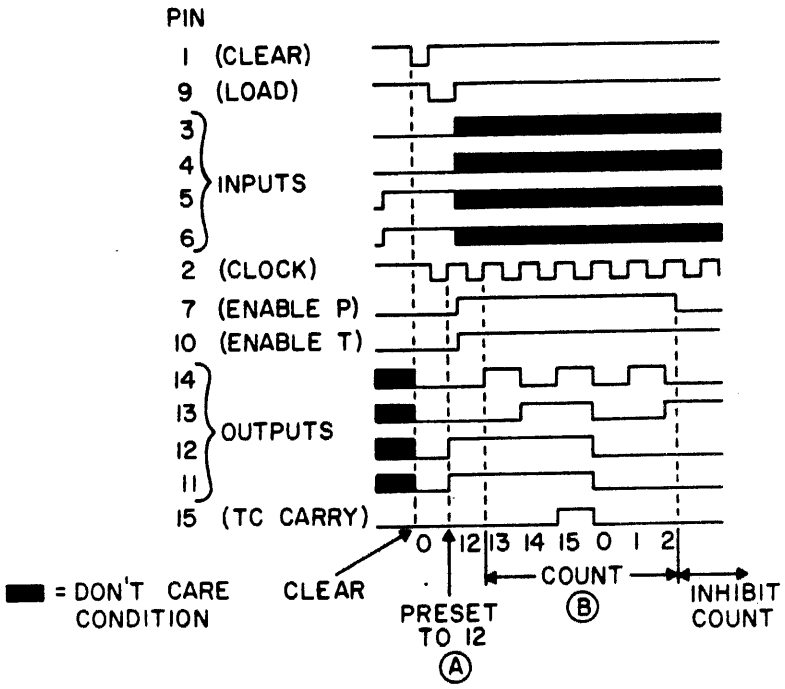
1. Vendor identification:

Element	Vendor Number
158	74161, 9316
158A	74161
158LS	74LS161

2 Package pin configuration.



158
Sheet 1 of 3



NOTES:

Ⓐ MODE SELECTION WITH POSITIVE-GOING CLOCK IS:

PINS 7 & 10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

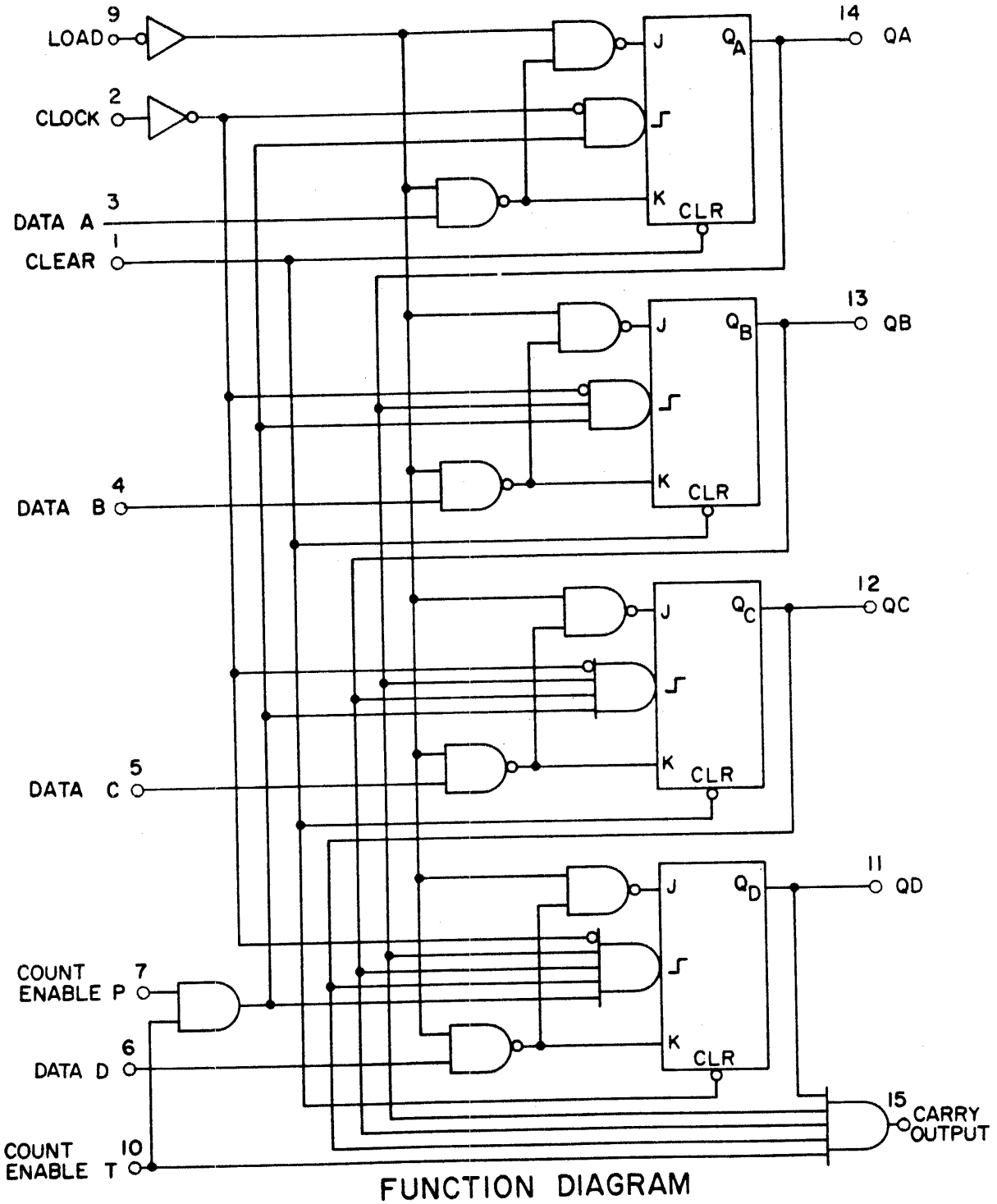
Ⓑ PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

Ⓒ ILLUSTRATED ABOVE IS THE FOLLOWING:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

Ⓓ

PIN(S)	FUNCTION
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

TIMING SEQUENCE



FUNCTION DIAGRAM

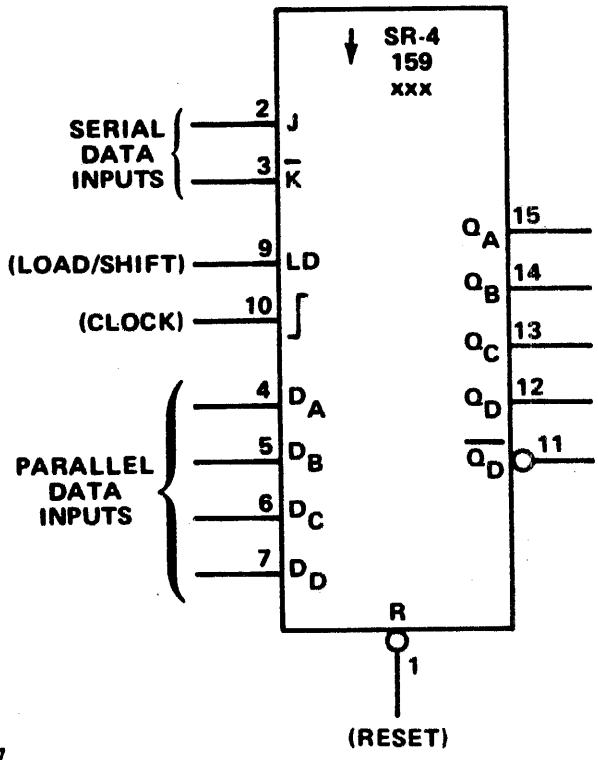
158
Sheet 3 of 3

DESCRIPTION

The 159 circuit is a synchronous 4-bit shift register capable of shifting, counting, storage, and serial code conversion.

Data entry is synchronous; the outputs change state after each low to high transition of the clock. When the load/shift input is low, the parallel inputs determine the next condition of the shift register. When the load/shift input is high, the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through the J-K (serial) inputs. By tying the J and K inputs together, D-type entry is obtained (see truth table).

A low level to the clear input will clear the outputs to a low level regardless of the levels to any input.



LOGIC SYMBOL

NOTES:

1. Vendor identification

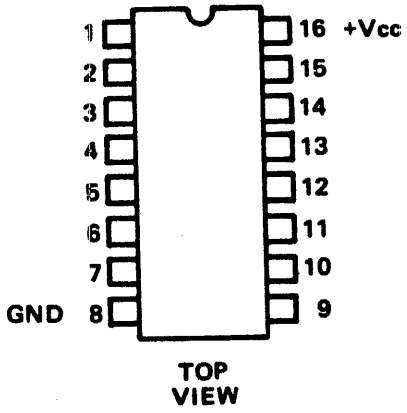
Element	Vendor Number
159	74195, 9300
159LS	74LS195

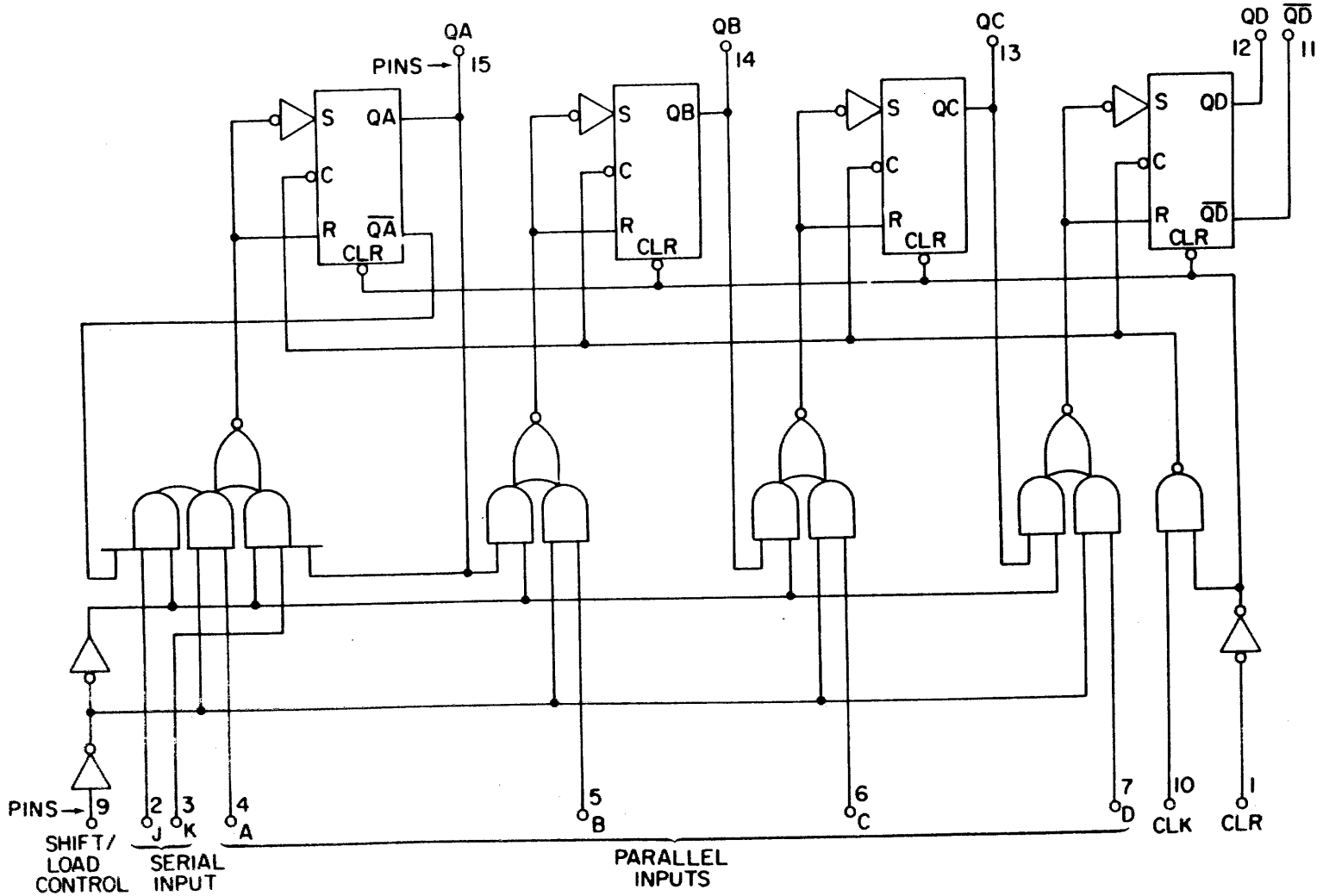
2. Pin Names

Pin	Function
1	Master Reset (clear)
2	First stage J input
3	First stage K input
4,5,6,7	Parallel data inputs
9	Load/Shift control
10	Clock
12,13, 14,15	Parallel outputs
11	Complementary output ($\overline{12}$) for last stage

INPUT PINS		OUTPUT PIN
2	3	15
0	0	0
0	1	0(NO CHANGE)
1	0	1 (TOGGLES)
1	1	1

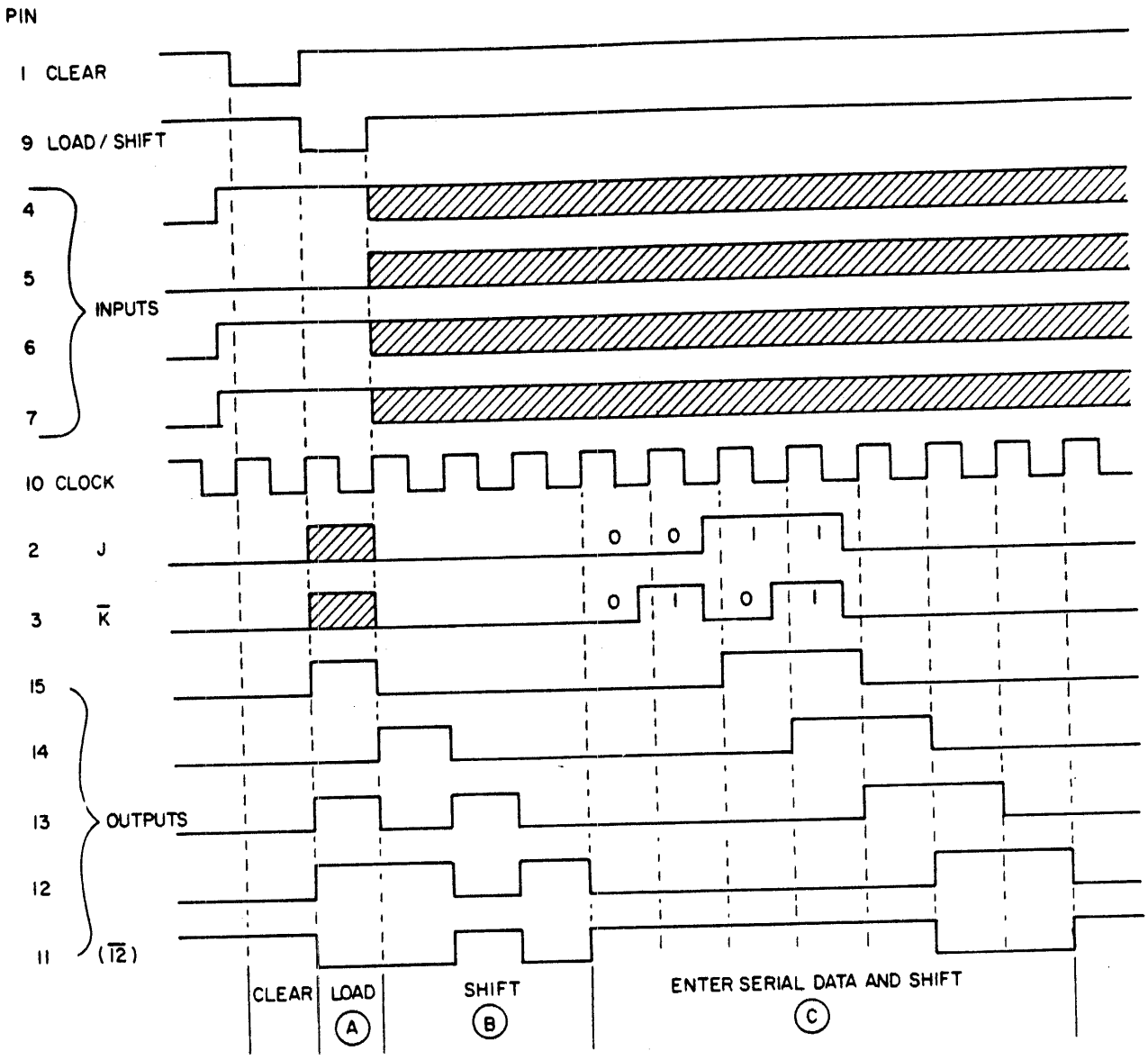
3. Package pin configuration.





FUNCTIONAL DIAGRAM

159
Sheet 3 of 4



NOTES:

(A) Parallel data entered via A,B,C,D inputs by pin 9 low and positive-going signal on pin 10.

(B) Data shifts down (Pin 15 ⟶ Pin 14, etc.) with clock.

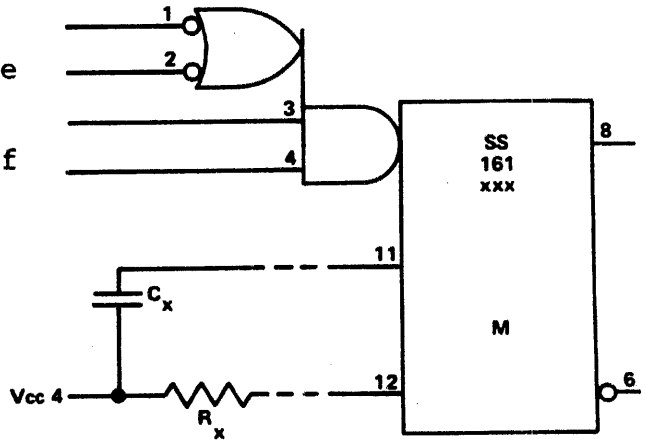
(C) Serial data entered into J-$\overline{K}$ inputs by pin 9 high and positive-going clock. Pin 4 input inhibited because pin 9 is high. Outputs follow Truth Table shown below. (Were J and $\overline{K}$ tied together, output at pin 15 would track the J input with no deviation from the Truth Table.)

159
Sheet 4 of 4

DESCRIPTION

The 161 circuit is a monostable retriggerable multivibrator that provides an output pulse whose duration is a function of external timing components.

Input pins 3 and 4 trigger on the positive going edge of the input pulse and pins 1 and 2 trigger on the negative going input pulse. The 161 circuit will retrigger while in the pulse timing state (pin 8 high); the end of the last pulse will be timed from the last input.



LOGIC SYMBOL

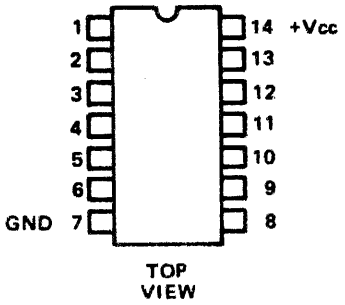
OUTPUT PULSE WIDTH (t) IS DEFINED AS FOLLOWS:

$$t = 0.32\ R_x\ C_x \left[1 + \frac{0.7}{R_x}\right]$$

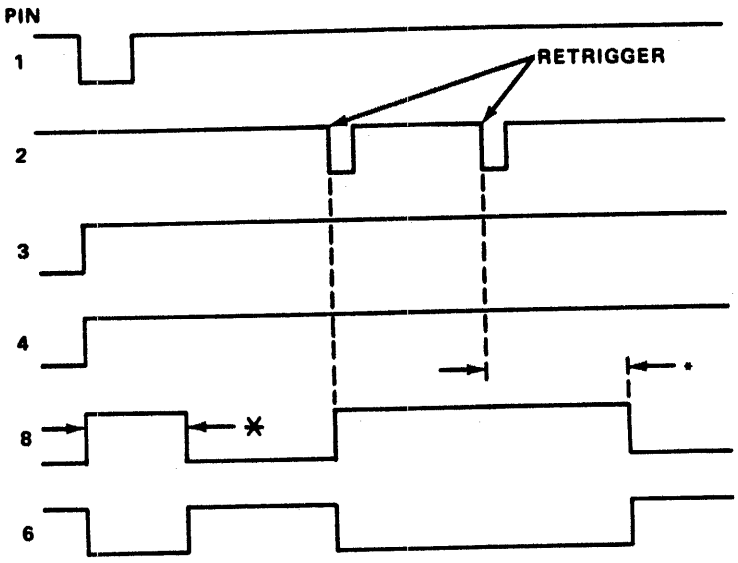
R_x IS IN kΩ, C_x IS IN pF, t IS IN ns

NOTES:

1. Substitute delay period for 'M'
2. Vendor identification: 9601
3. Package pin configuration.



TOP VIEW



*PULSE WIDTH DETERMINED BY RC TIMING NETWORK

TIMING SEQUENCE

TRUTH TABLE

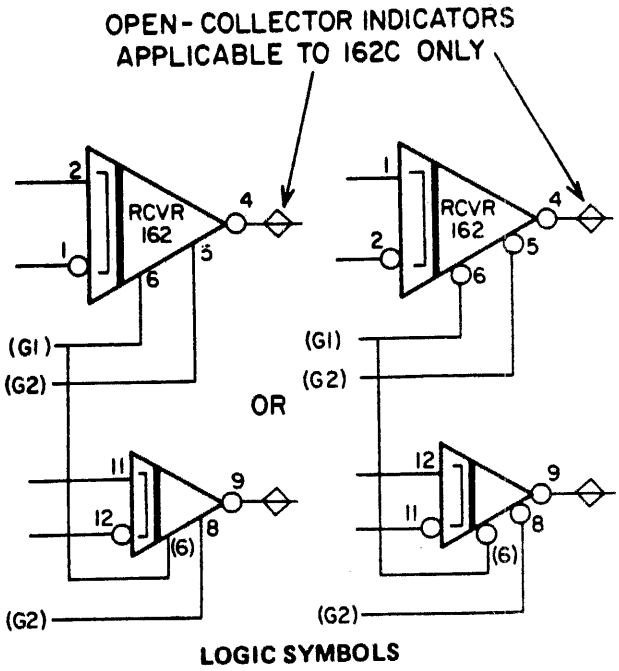
INPUT PINS				OPERATION	OUTPUT PINS	
1	2	3	4		8	6
H→L	H	H	H	TRIGGER	⊓	⊔
H	H→L	H	H	TRIGGER	⊓	⊔
L	X	L→H	H	TRIGGER	⊓	⊔
X	L	L→H	H	TRIGGER	⊓	⊔
L	X	H	L→H	TRIGGER	⊓	⊔
X	L	H	L→H	TRIGGER	⊓	⊔
H	H	H	H		L	H
X	X	L	X		L	H
X	X	X	L		L	H

X = DON'T CARE

161
Sheet 2 of 2

DESCRIPTION

The 162 circuit is a dual differential line receiver. A minimum differential voltage of 25 mV is required to ensure a high or low output level. Common mode voltages of ±3 V or less will be rejected. The minimum allowable differential input voltage is 5 volts. The 162C features open-collector outputs.



LOGIC SYMBOLS

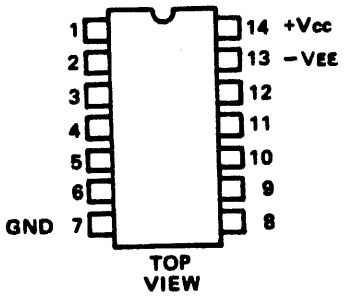
NOTES:

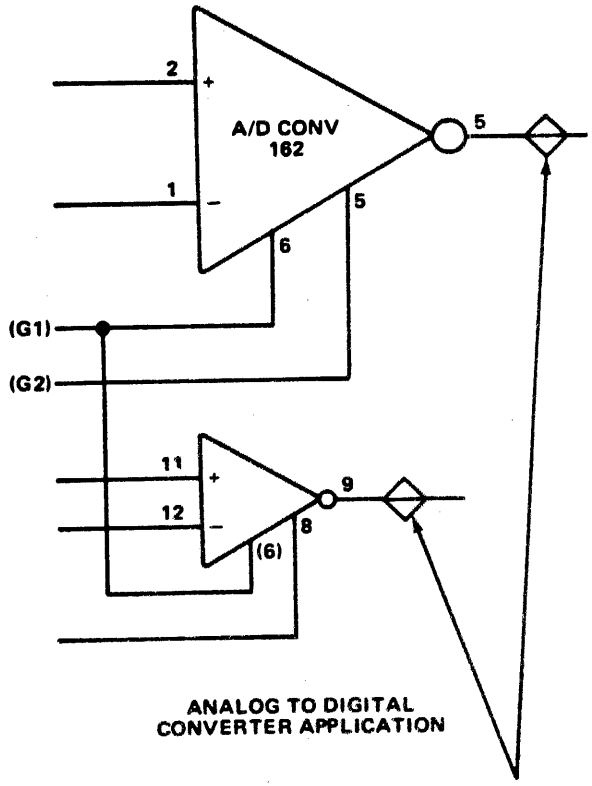
1. The two sections may be shown separately by duplicating pin 6 in the second section.

2. Vendor identification:

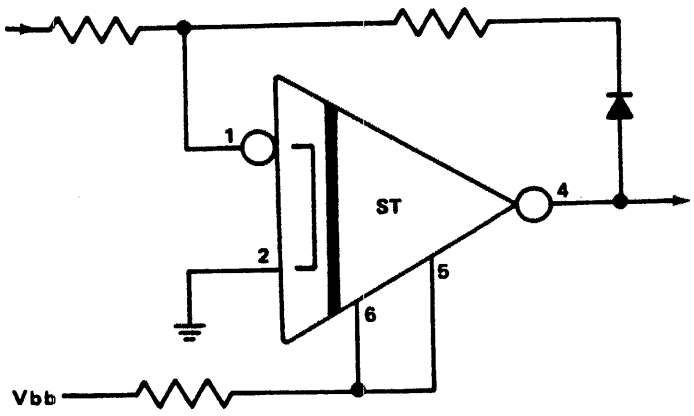
Element	Vendor Number
162	75107
162C	75108
162S	NE521F

3. Package pin configuration.

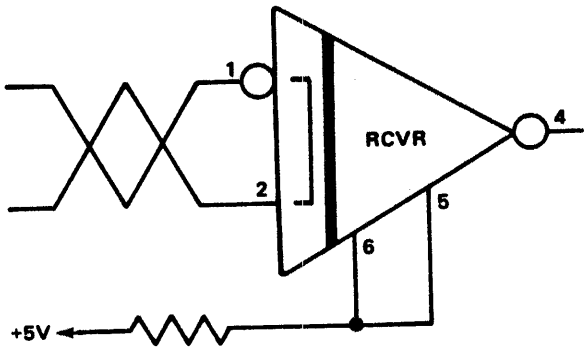




ANALOG TO DIGITAL
CONVERTER APPLICATION



I62 DUAL DIFFERENTIAL RECEIVER USED AS A SCHMITT TRIGGER WITH EXTERNAL FEEDBACK NETWORKS AND FIXED BIAS ENABLING G1 AND G2 STROBE INPUTS'

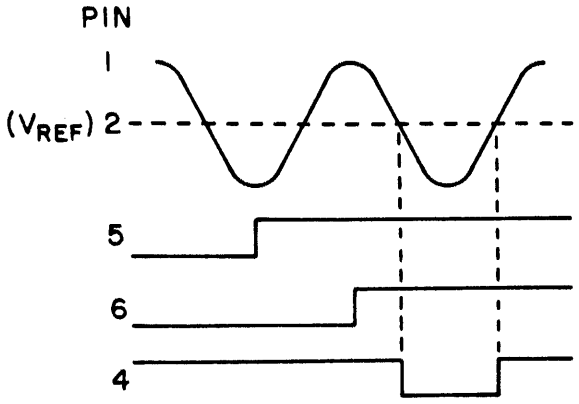


TWISTED PAIR RECEIVER APPLICATION

DIFFERENTIAL INPUTS	STROBES		OUTPUT
	G1	G2	
$V_{ID} \geq 25MV$	L OR H	L OR H	H
$-25MV < V_{ID} < 25MV$	L OR H	L	H
	L	L OR H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25MV$	L OR H	L	H
	L	L OR H	H
	H	H	L

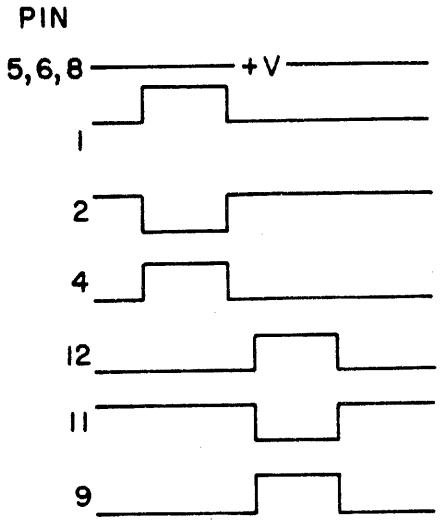
THE DIFFERENTIAL INPUT VOLTAGE POLARITIES SHOWN MEASURED AT PIN A WITH RESPECT TO PIN B. A MINUS POLARITY INDICATES THAT PIN A IS MORE NEGATIVE THAN PIN B.

TRUTH TABLE
(RCVR APPLICATION)

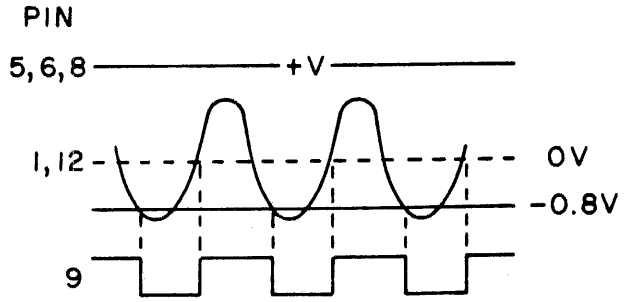


PIN 4 IS LOW ONLY IF G1 AND G2 ARE HIGH AND PIN 1 IS MORE NEGATIVE THAN PIN 2. G2 IS COMMON TO BOTH CONVERTERS.

162 DIGITAL TO ANALOG CONVERTER APPLICATION



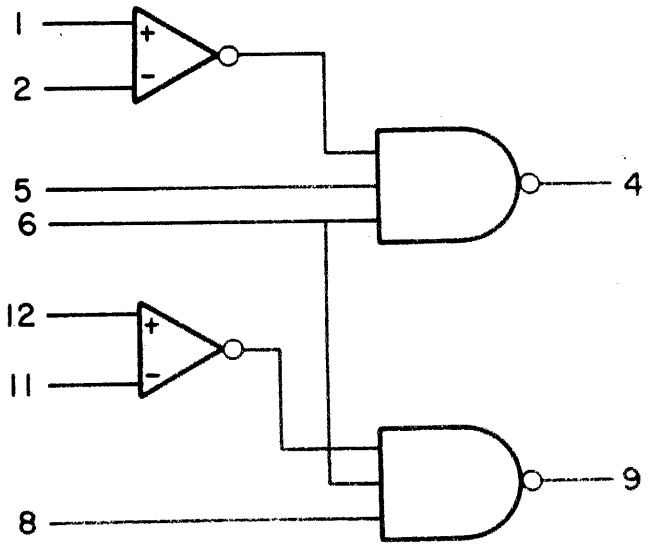
162 TWISTED PAIR RECEIVER APPLICATION



162 SCHMITT TRIGGER

TIMING SEQUENCE

FUNCTION DIAGRAM

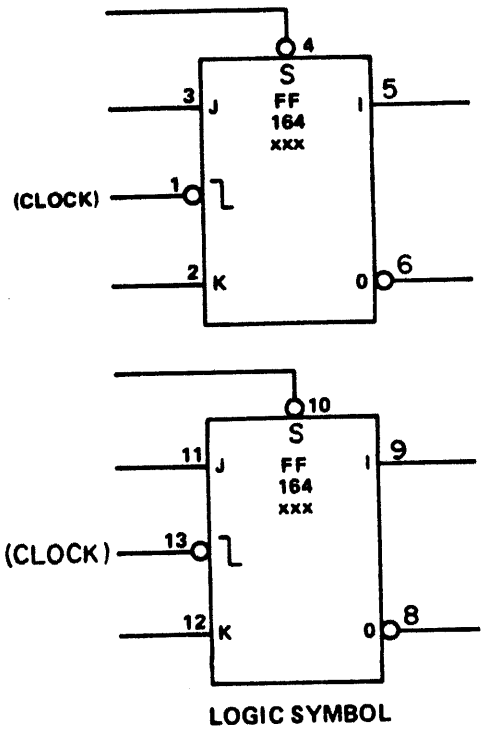


162
Sheet 3 of 3

DESCRIPTION

The 164 circuit is a dual negative-edge-triggered JK flip-flop. Each flip-flop is provided with a direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions.

Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the set-up and hold-times. The inputs are inhibited when the clock is low and enabled when the clock rises. The JK inputs continuously respond to input information when the clock is high. The data state at the inputs throughout the interval between set-up and hold time is stored in the flip-flop when the clock pulse goes low. Each flip flop may be set at any time without regard to the clock state by applying a low level to the SET input.



LOGIC SYMBOL

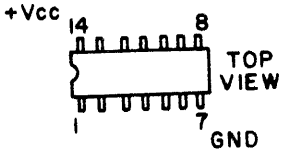
NOTES:

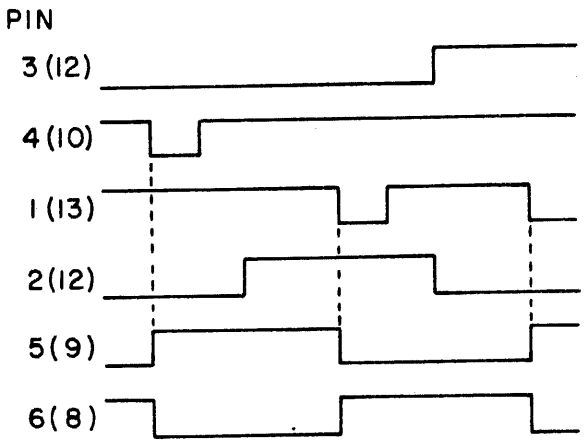
1. Symbol repeated for each flip-flop.

2. Vendor identification:

Element	Vendor Number
164H	3062
164S	74S113

3. Package pin configuration.





TIMING SEQUENCE

INPUT		OUTPUT BEFORE CLK		OUTPUT BEFORE CLK	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

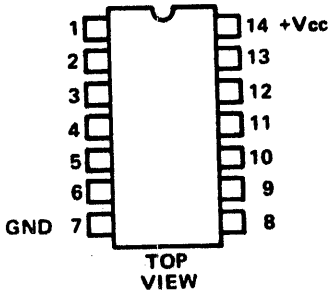
TRUTH TABLE

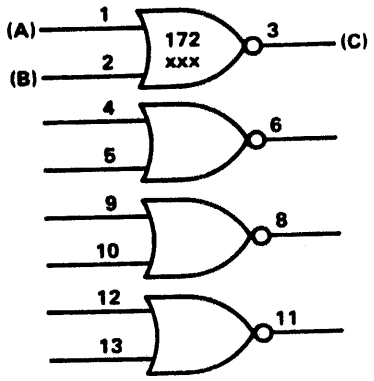
DESCRIPTION

The 172H circuit is a quad, 2-input, positive NOR gate.

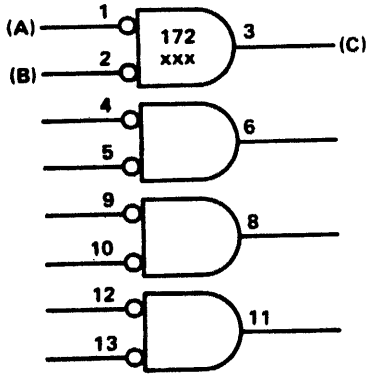
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 3002
3. Package pin configuration.





OR



LOGIC SYMBOL

A	B	C
L	L	H
H	L	L
L	H	L
H	H	L

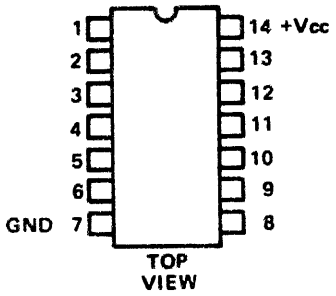
TRUTH TABLE

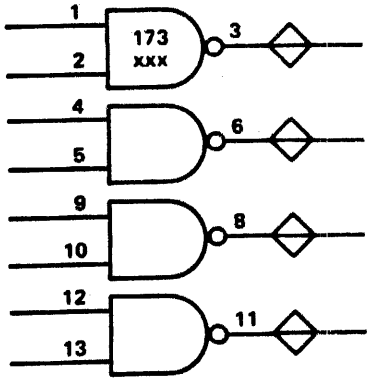
DESCRIPTION

The 173H circuit is a quad, 2-input, positive NAND gate with an open collector output.

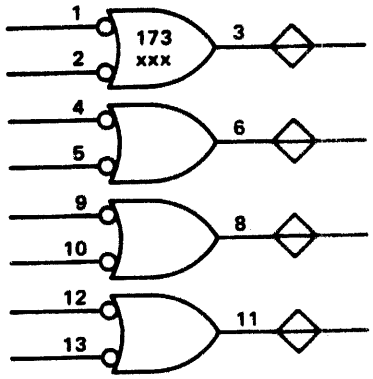
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 3004
3. The output of each gate is an open collector.
4. Package pin configuration.





OR



LOGIC SYMBOL

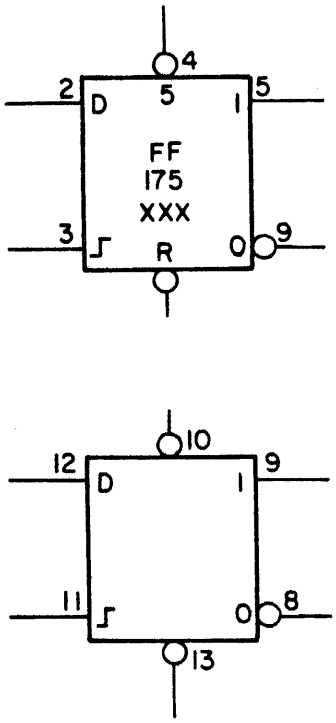
A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

TRUTH TABLE

DESCRIPTION

The 175 circuit is a dual, positive-edge-triggered, D-type flip-flop. This device consists of two completely independent D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register application.

Information at input CD is transferred to output Q (pin 5/9) on the positive-going edge of the clock pulse. Clock pulse triggering occurs at a voltage level of the pulse and is not directly related to the transition time of the positive-going pulse. When the clock is at either the high or low level, the CD-input signal has no effect.



LOGIC SYMBOL

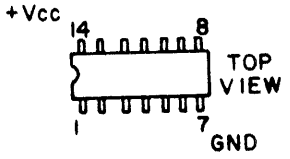
NOTES:

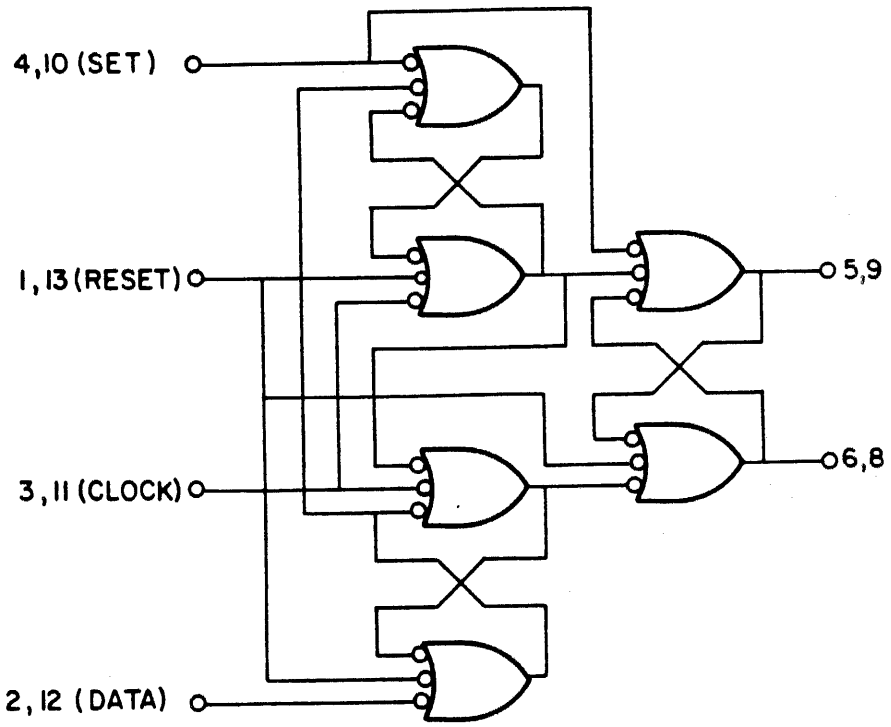
1. Symbol repeated for each flip-flop.

2. Vendor identification:

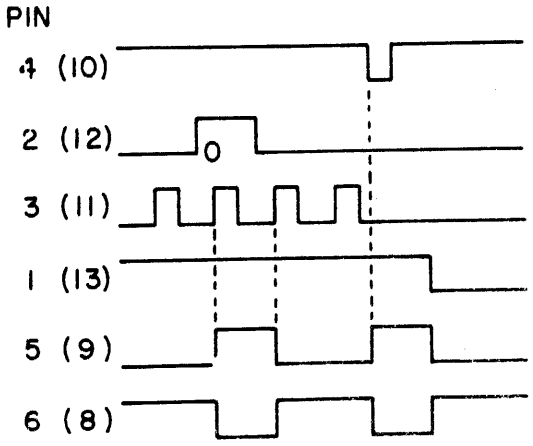
Element	Vendor Number
175	7474
175LS	74LS74
175S	74S74

3. Package pin configuration.





FUNCTION DIAGRAM
(EACH FLIP-FLOP)



TIMING SEQUENCE

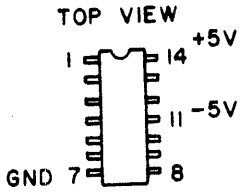
DESCRIPTION

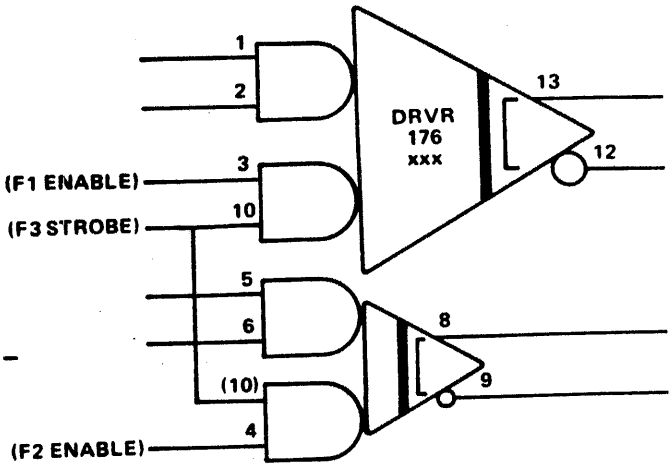
The 176 circuit is a dual differential line driver. This circuit accepts a DTL or TTL logic signal and transmits it over a differential line pair. "On" state output current is typically 12 mA. "Off" state output current is 100 µA max. The output common mode voltage range is -3 V to +10 V with respect to the circuit ground.

NOTES:

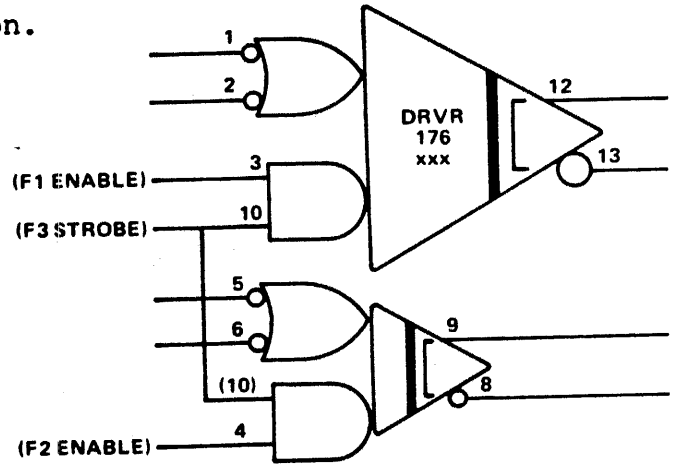
1. Type 176 Vendor identification: 75110

2. Package pin configuration.

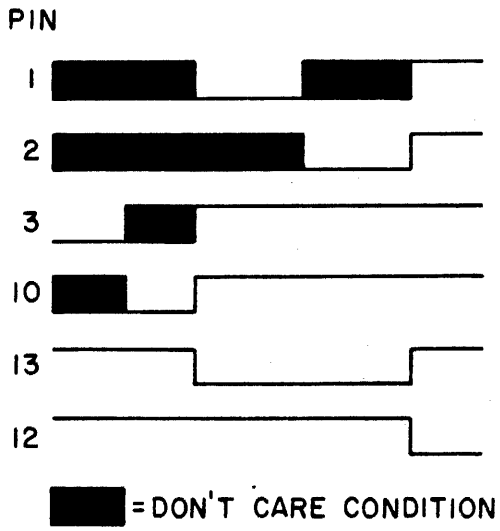




OR



LOGIC SYMBOL



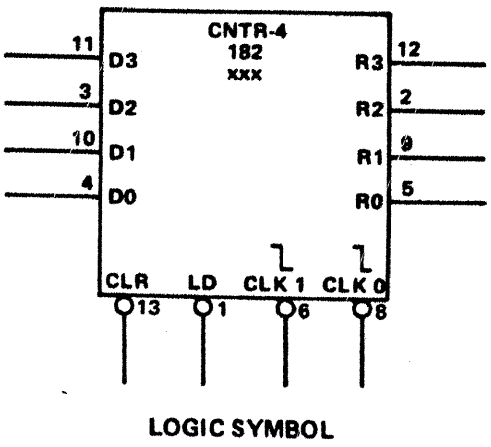
TIMING SEQUENCE

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS *		OUTPUT CONDITION
1, 5	2, 6	3, 4	10	9, 12	8, 13	
1 OR 0 1 OR 0	1 OR 0 1 OR 0	0 1 OR 0	1 OR 0 0	1 1	1 1	INHIBITED
0 1 OR 0 1	1 OR 0 0 1	1 1 1	1 1 1	1 1 0	0 0 1	ACTIVE DATA STATE

* LOW OUTPUT REPRESENTS THE CURRENT ON STATE.
HIGH OUTPUT REPRESENTS THE CURRENT OFF STATE.

TRUTH TABLE

is a 4-bit bi-
uring the count
ransfer of in-
e ouputs occurs
e-going edge of
e. The direct
), when taken low,
puts low regardless
s of the clocks
6). The 182 is
ammable; that is,
may be preset to
by placing a low
the count/load input
and entering the de-
ta at the inputs. The
will then change to
the data inputs in-
of the state of the
inputs. This allows the
o be used as a 4-bit latch
ster application) by in-
vating the clock inputs and
ng the count/load input as a
a strobe.



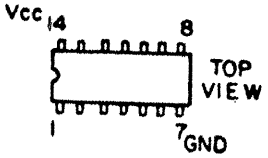
LOGIC SYMBOL

OTES:

1. Vendor identification:

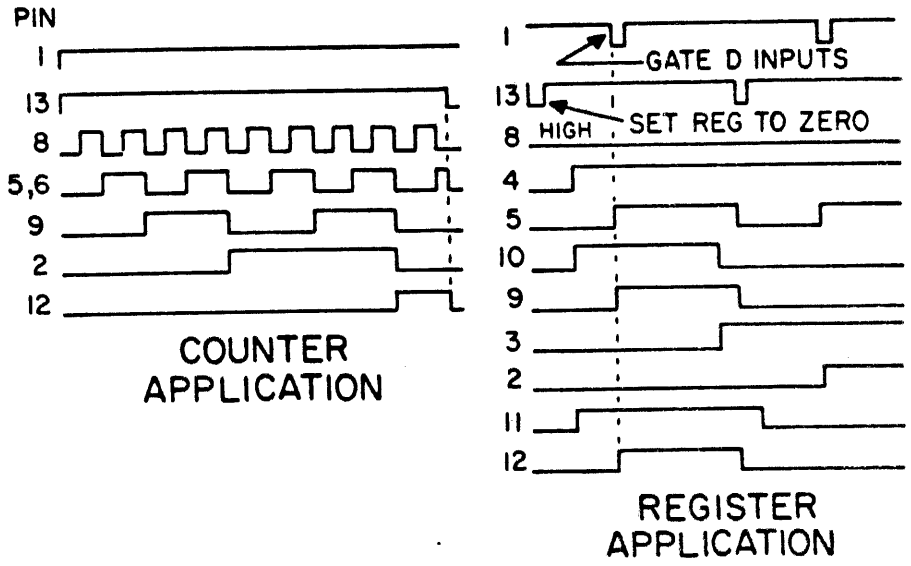
Element	Vendor Number
182	74197, 8291
182S	82S91

2. Package pin configuration.



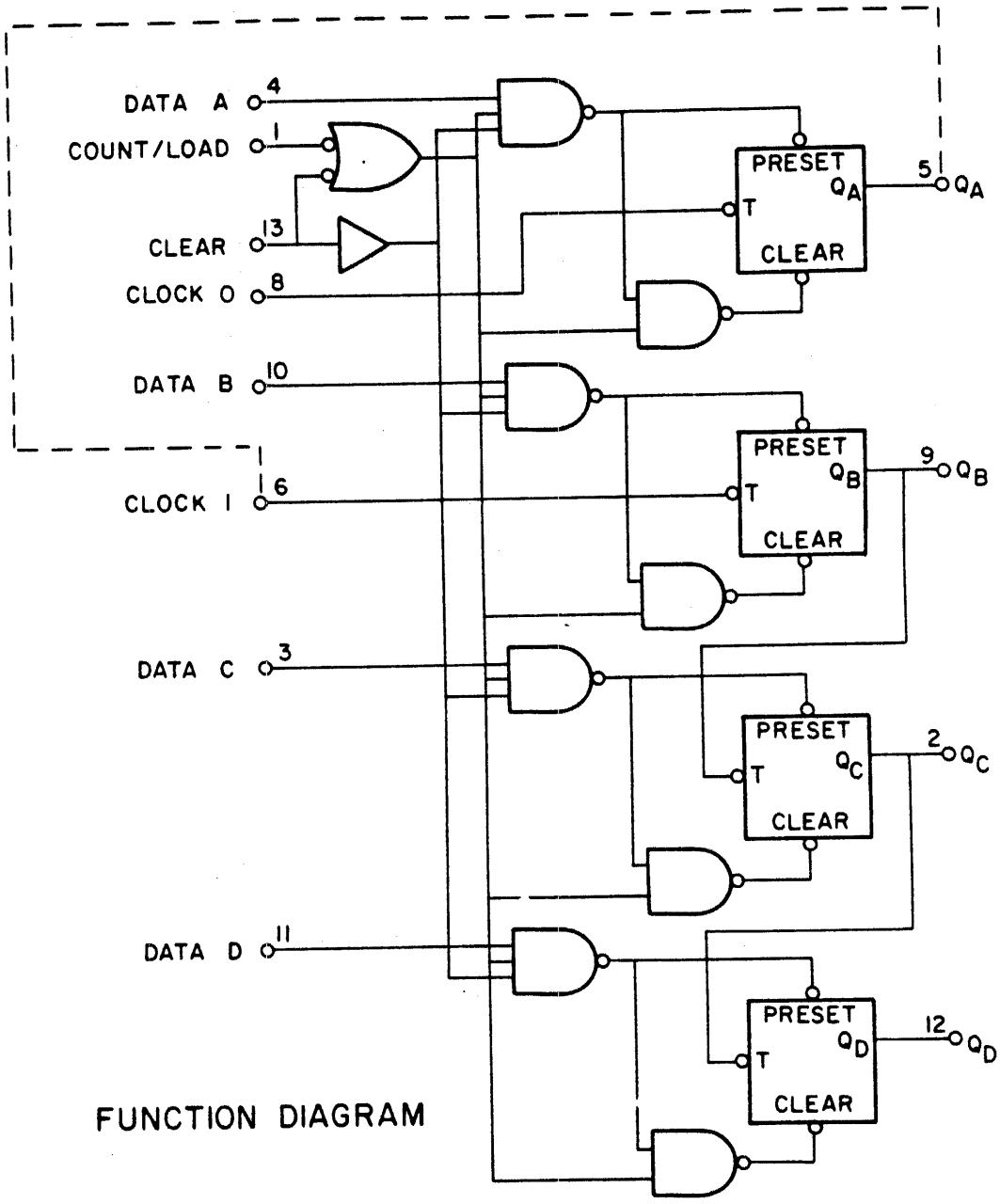
COUNT	OUTPUT			
	R3	R2	R1	R0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TRUTH TABLE
(WITH PINS 5 AND 6 WIRED TOGETHER)



TIMING SEQUENCE

Connect pins 5 & 6 for 4-bit counting, using data input A. As a 3-Bit counter, data input B is used. First stage may then be used as an independent data latch if count/load and Clear Functions coincide with those of the counter.



FUNCTION DIAGRAM

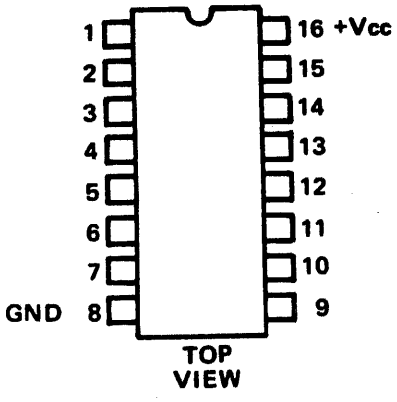
182
Sheet 3 of 3

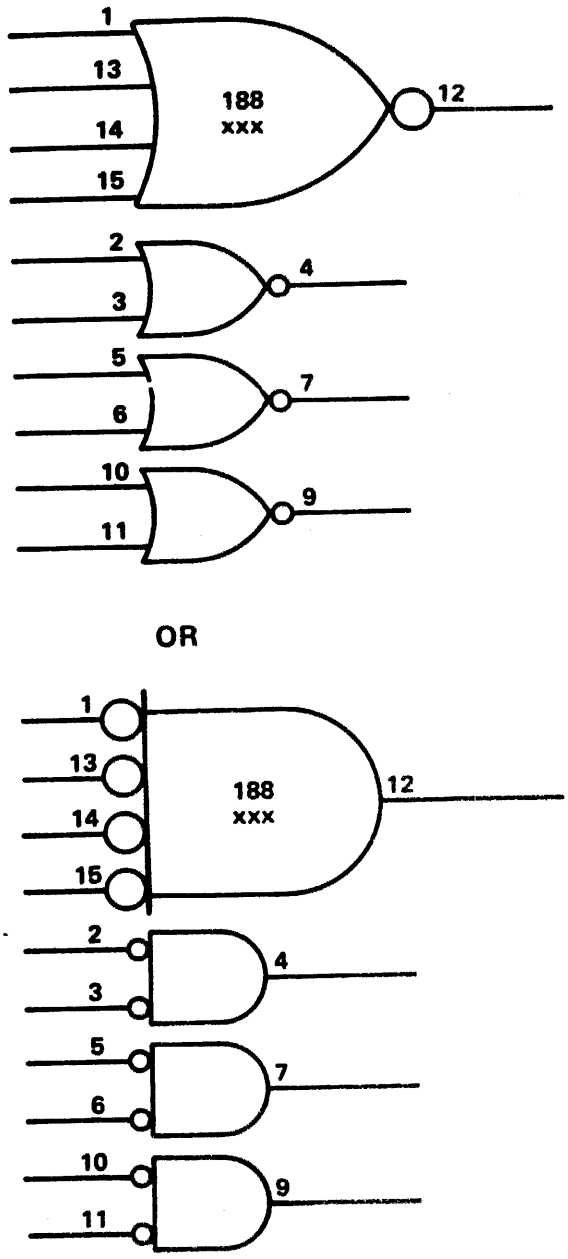
DESCRIPTION

The 188 circuit consists of one 4-input and three 2-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 9015
3. Package pin configuration.





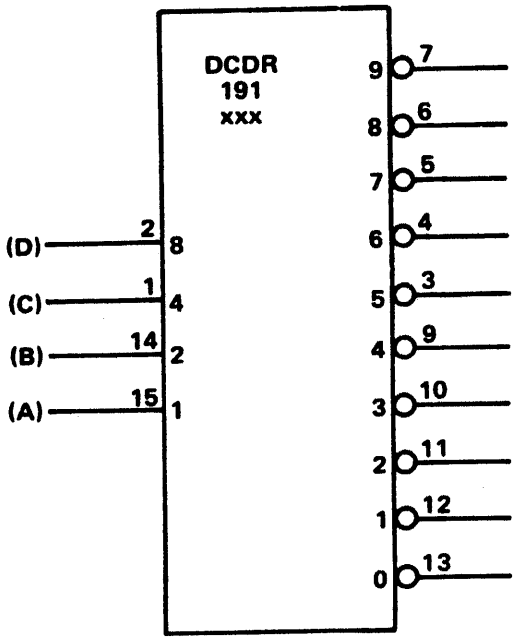
LOGIC SYMBOL

188
Sheet 1 of 1

DESCRIPTION

Circuit type 191 is a BCD-to-decimal (1-of-10) decoder. Four active-high BCD inputs provide one of ten mutually exclusive active-low outputs. When a binary code greater than 9 is applied, all outputs are high. This facilitates BCD to decimal conversions and eight-channel demultiplexing and decoding.

The 191 circuit can serve as a one-of-eight decoder with the D input acting as the active-low enable. Eight-channel demultiplexing then results when the desired output is addressed by inputs A, B, and C.

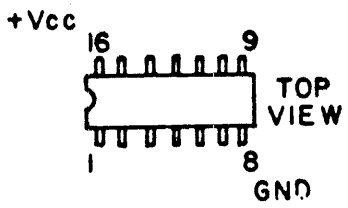


LOGIC SYMBOL

NOTES:

1. Vendor identification: 9301

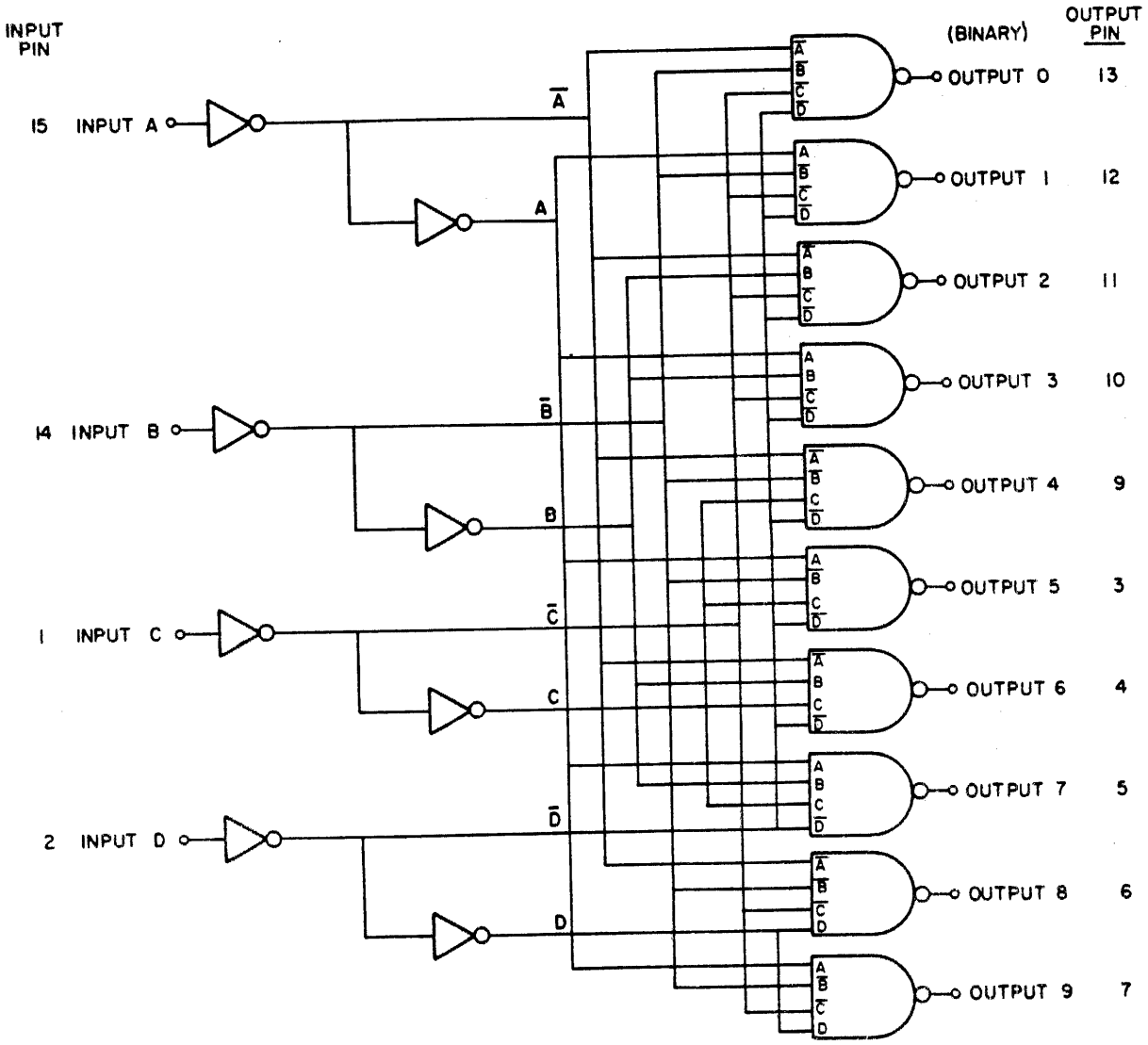
2. Package pin configuration.



INPUT PIN				LO ("0") OUTPUT PIN, OTHER OUTPUTS = "1"
2	1	14	15	
0	0	0	0	13
0	0	0	1	12
0	0	1	0	11
0	0	1	1	10
0	1	0	0	9
0	1	0	1	3
0	1	1	0	4
0	1	1	1	5
1	0	0	0	6
1	0	0	1	7
1	0	1	0	*
1	0	1	1	*
1	1	0	0	*
1	1	0	1	*
1	1	1	0	*
1	1	1	1	*

* = ALL OUTPUT PINS HIGH

TRUTH TABLE



FUNCTION DIAGRAM

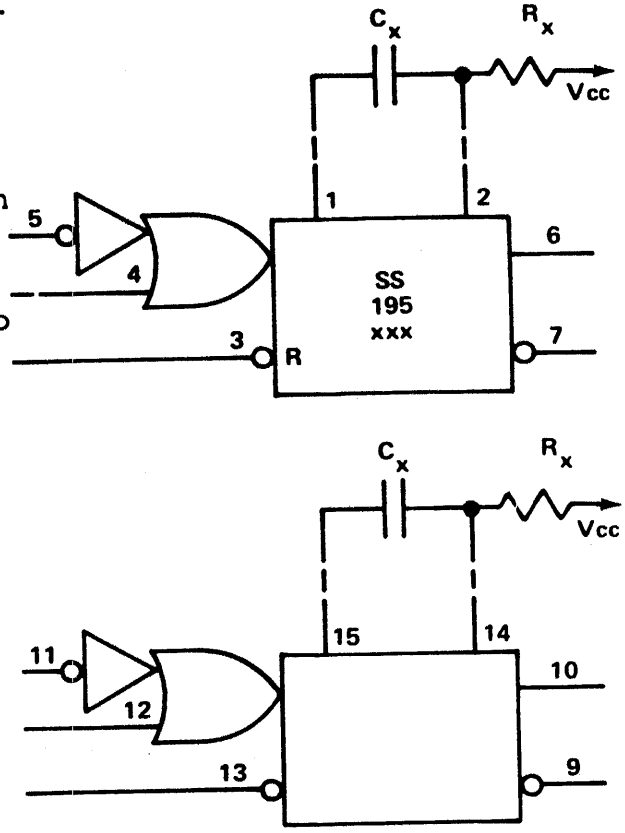
191
Sheet 2 of 2

DESCRIPTION

The 195 circuit is a dual retriggerable monostable multivibrator. Input pins 4 and 12 trigger on the positive-going edge of the input pulse and pins 5 and 11 trigger on the negative-going edge. The 195 circuit will retrigger while in the pulse timing state (pin 3/13 high) and the end of the last pulse will be timed from the last input. A low level to the reset input (pin 3/13) resets pin 6/10 to low level and inhibits data inputs.

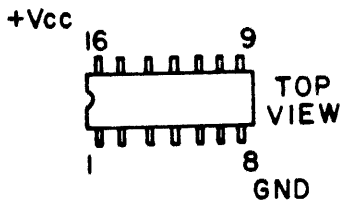
NOTES:

1. The full timing network would be shown on the logic diagram.
2. Vendor identification: 9602



LOGIC SYMBOL

3. Package pin configuration:



4. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high level pulse, ⎎ = one low level pulse, x = irrelevant (any input, including transitions).

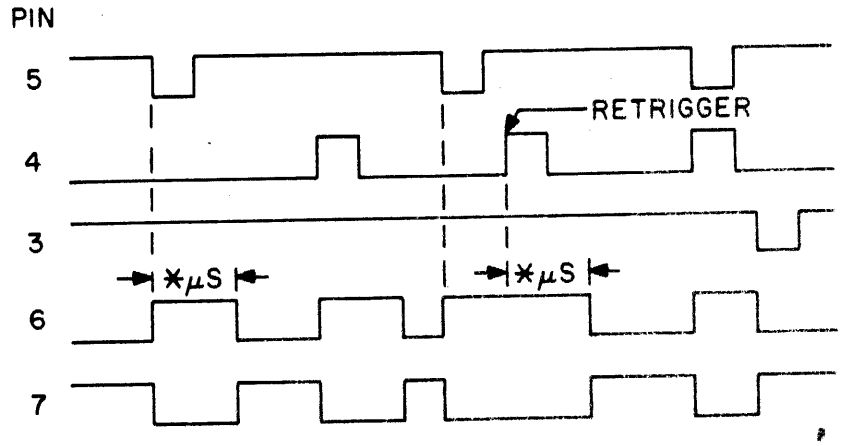
INPUT PINS			OUTPUT PINS	
5(11)	4(12)	3(13)	6(7)	10(9)
↓	L	H	⎍	⎍
H	↑	H	⎍	⎍
X	X	L	L	H

TRUTH TABLE
(SEE NOTE 4)

5. Output pulse width (†) is defined as follows:

$$\dagger = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X})$$

R_X is in kΩ, C_X is in pF
† is in ns



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.

TIMING SEQUENCE

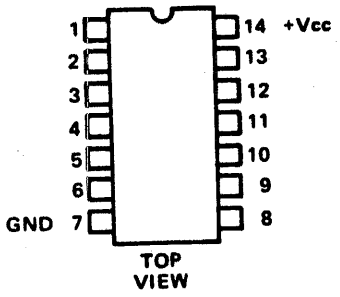
195
Sheet 2 of 2

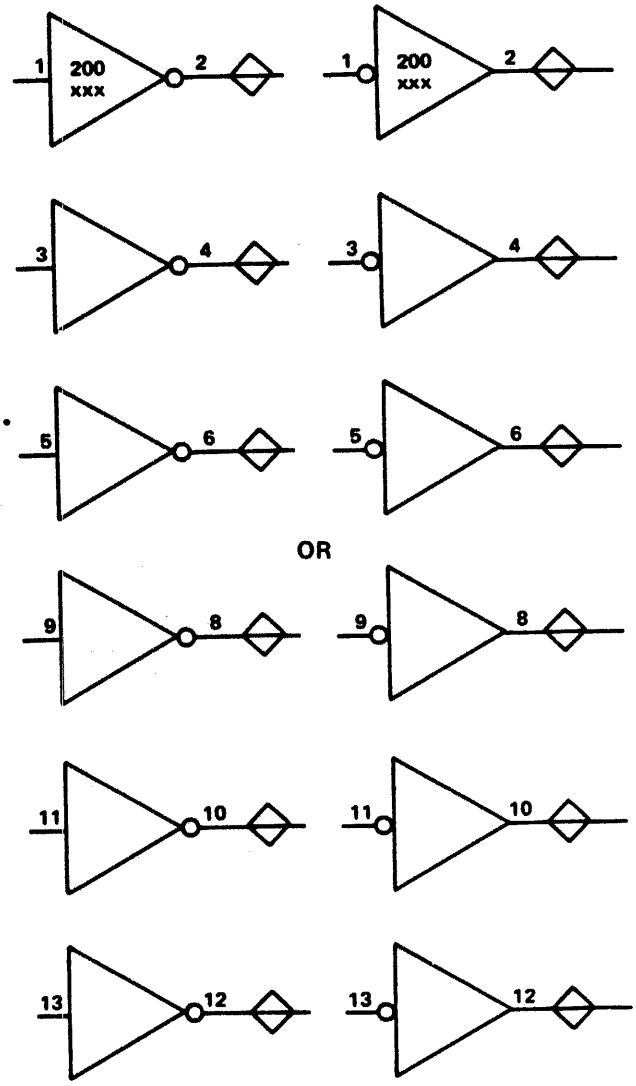
DESCRIPTION

The 200 circuit is a hex inverter buffer/driver with an open-collector output.

NOTES:

1. Symbol sections may be shown separately.
2. Vendor identification: 7406
3. Package pin configuration.





LOGIC SYMBOL

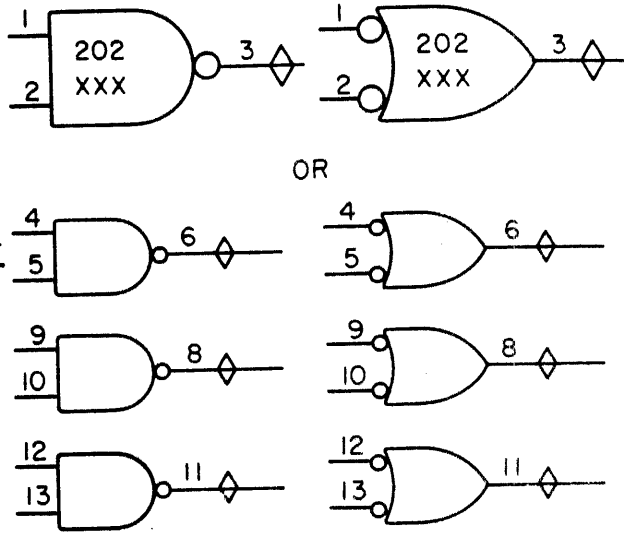
200
Sheet 1 of 1

DESCRIPTION

The 202 circuit is a quad, 2-input, positive NAND gate with open-collector outputs.

NOTES:

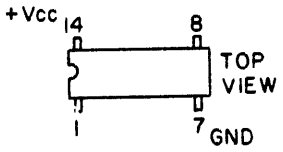
1. Symbol sections may appear separately.



2. Vendor identification:

Element	Vendor Number
202	7403
202H	74H01
202LS	74LS03
202S	74S03

3. Package pin configuration.



INPUTS		OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

TRUTH TABLE
(EACH GATE)

202
Sheet 1 of 1

DESCRIPTION

Type 208 is a dual, 4-input, positive NAND gate.

NOTES

1. Symbol sections may appear separately.

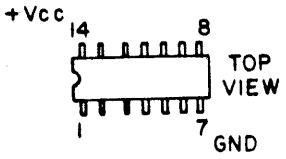
2. Vendor identification:

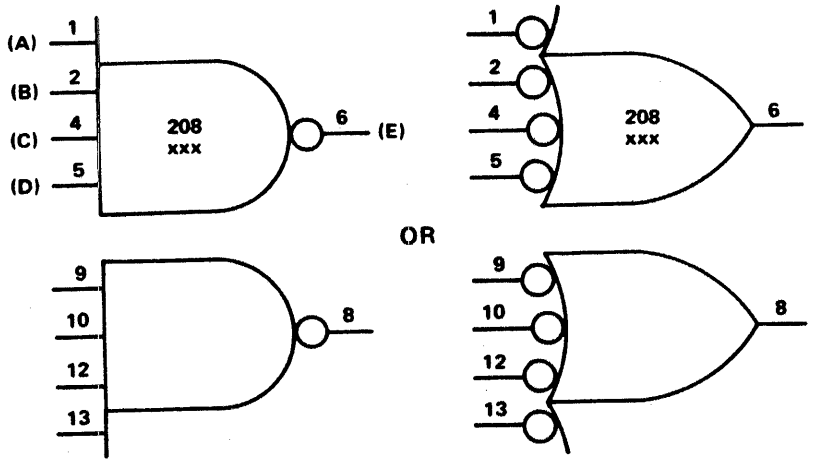
Element	Vendor Number
208	7420
208H	74H20
208L	74L20
208LS	74LS20
208S	74S20

3. Package pin configuration.

INPUTS				OUTPUT
A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE





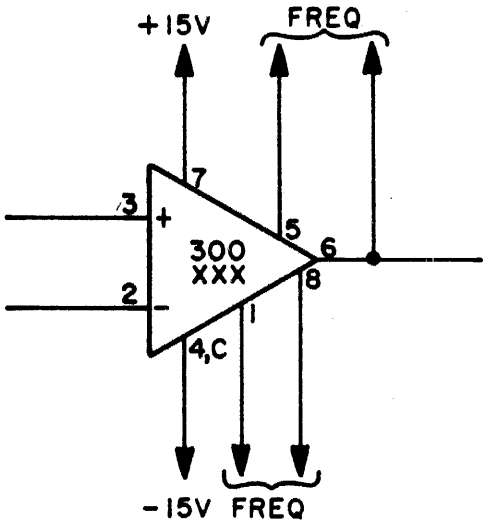
LOGIC SYMBOL

208
Sheet 1 of 1

DESCRIPTION

Element 300 is a high-gain operational amplifier mounted on a single chip.

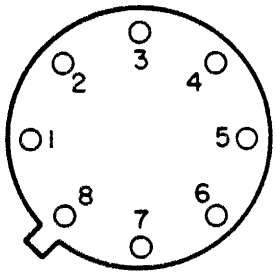
Pin	Function
1	Input Frequency Comp.
2	Inverting Input
3	Non-inverting Input
4	-V (Connected to Case)
5	Output Frequency Comp.
6	Output
7	+V
8	Input Frequency Comp.



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 709C



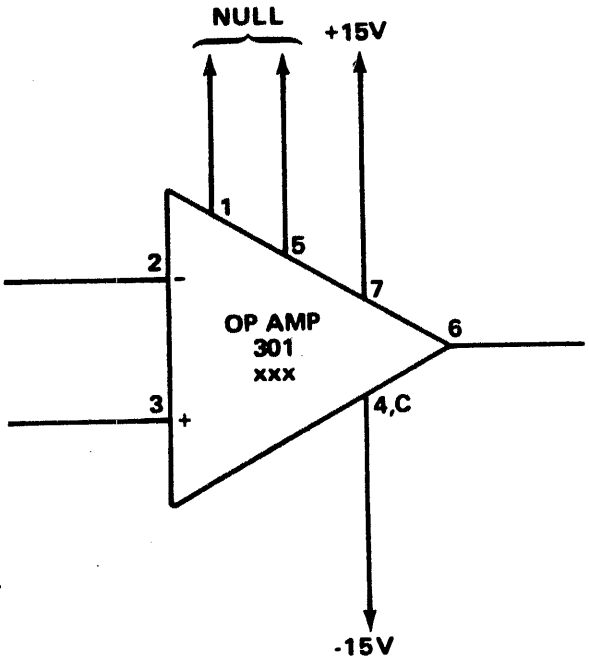
PACKAGE PIN CONFIGURATION

300
Sheet 1 of 1

DESCRIPTION

Element 301 is a frequency compensated, high gain, operational amplifier.

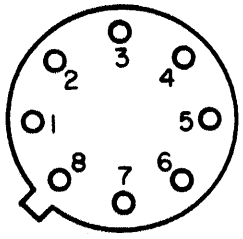
Pin	Function
1	Offset Null
2	Inverting Input
3	Non-inverting Input
4	-V
5	Offset Null
6	Output
7	+V
8	Not Used (no connection)



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 741C

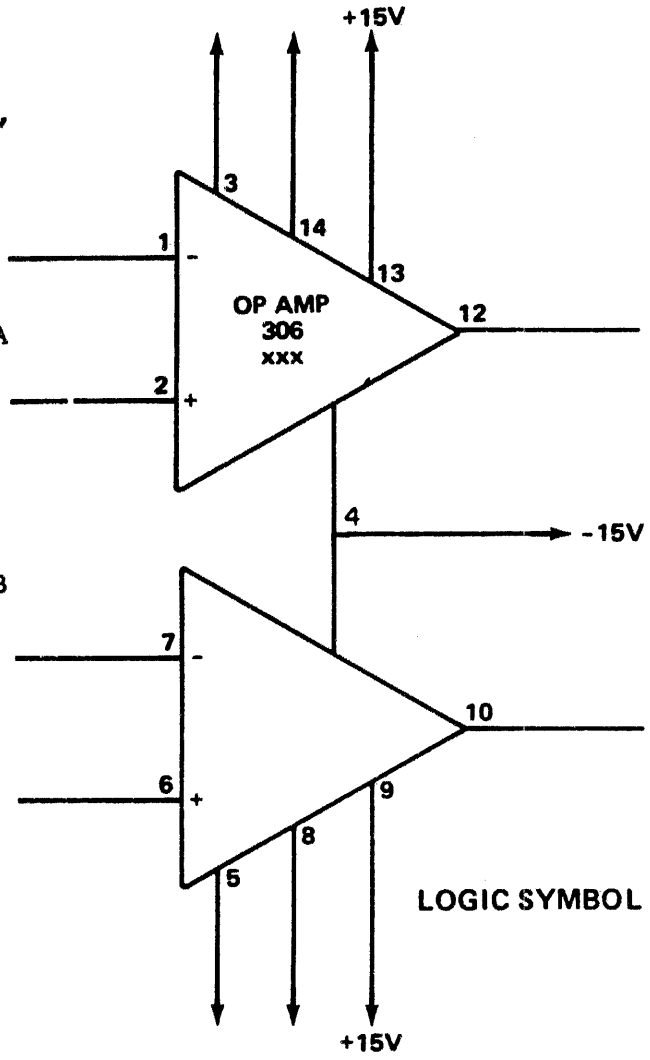


PACKAGE PIN CONFIGURATION

DESCRIPTION

Element 306 is a pair of frequency compensated, high gain, operational amplifiers.

Pin	Function
1	Inverting Input A
2	Non-inverting Input A
3	Offset Null A
4	-V
5	Offset Null B
6	Non-inverting Input B
7	Inverting Input B
8	Offset Null B
9	+V (B)
10	Output B
11	No Connections
12	Output A
13	+V (A)
14	Offset Null A

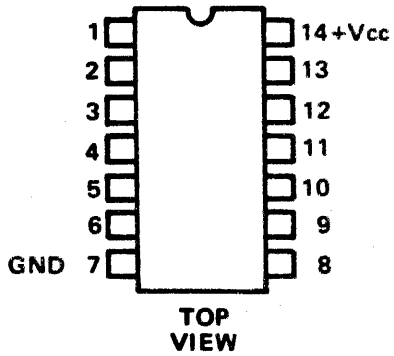


LOGIC SYMBOL

NOTES:

1. Separated sections have pin 4 (-15 V) shown in parentheses for second section.

2. Vendor Identification: 747C



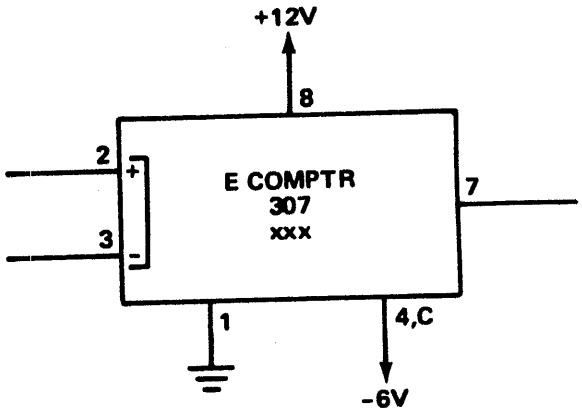
PACKAGE PIN CONFIGURATION

306
Sheet 1 of 1

DESCRIPTION

Element 307 is a differential voltage comparator.

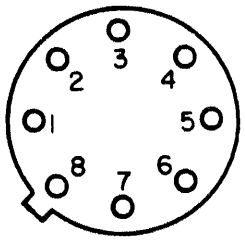
Pin	Function
1	GND
2	Non-inverting Input
3	Inverting Input
4	-V
5	No Connection
6	No Connection
7	Output
8	+V



LOGIC SYMBOL

NOTES:

1. Vendor Identification: 710



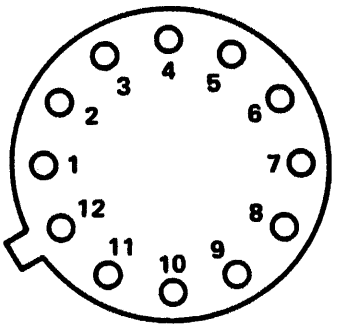
PACKAGE PIN CONFIGURATION

DESCRIPTION

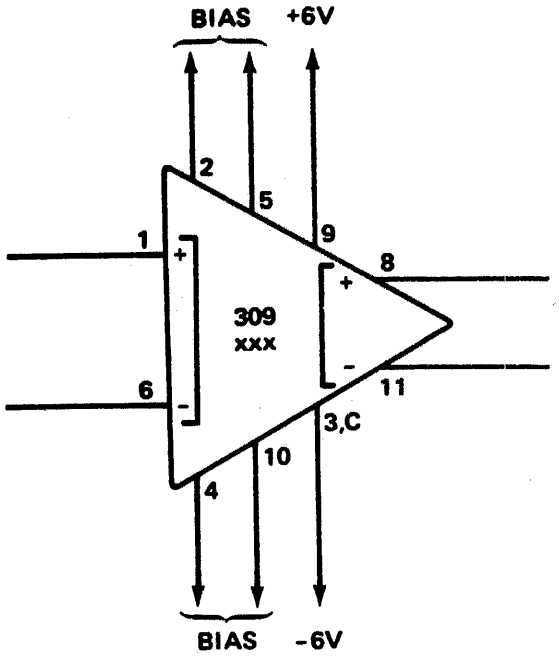
Element 309 is a wide-band differential amplifier with a nominal voltage gain of 9.

NOTES:

1. Vendor identification: 3001



PACKAGE PIN CONFIGURATION



LOGIC SYMBOL

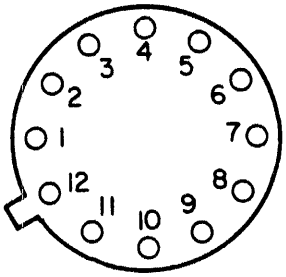
DESCRIPTION

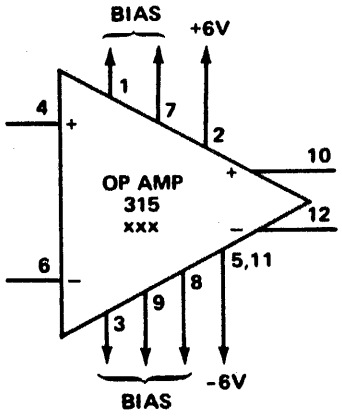
Element 315 is a wide-band amplifier for frequencies up to 200 MHz.

NOTES:

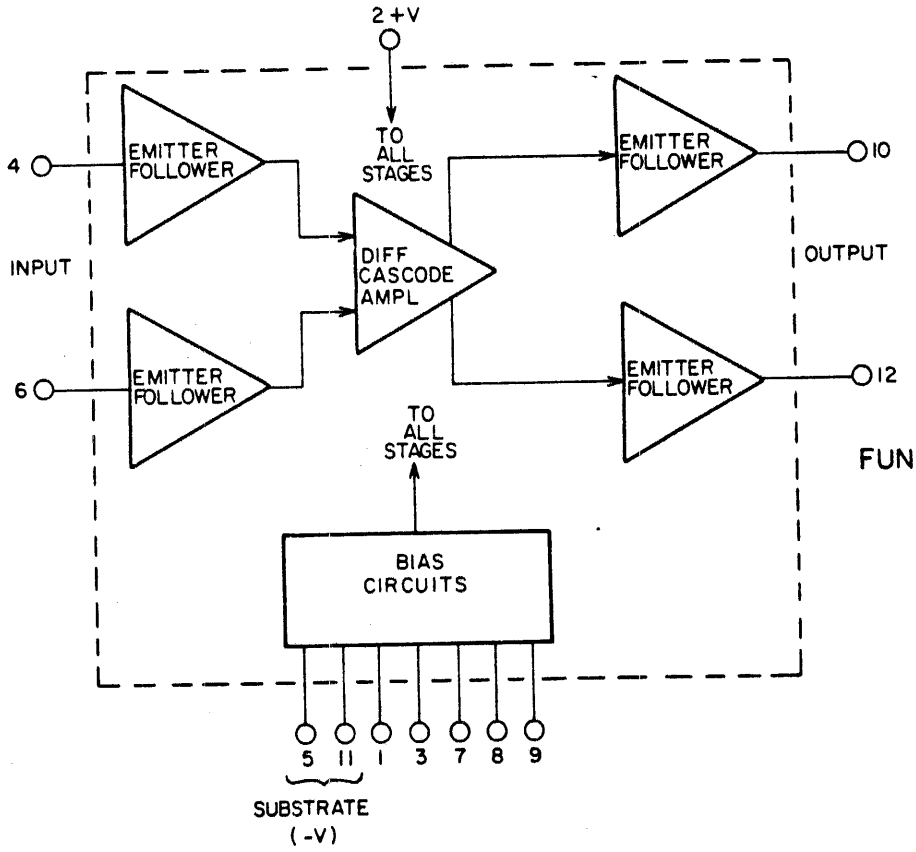
1. Vendor identification: CA3040

2. Package pin configuration:





LOGIC SYMBOL



FUNCTIONAL DIAGRAM

315
Sheet 1 of 1

DESCRIPTION

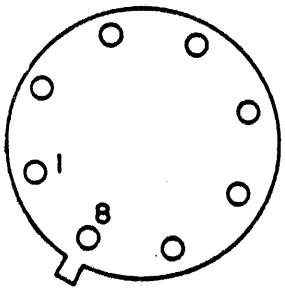
Element 316 is a wide band, unity-gain current amplifier capable of providing peak currents of ±200 mA into a 50-ohm load. The symmetrical class-B output provides a constant low output impedance for both the positive and negative slopes of the output pulses.

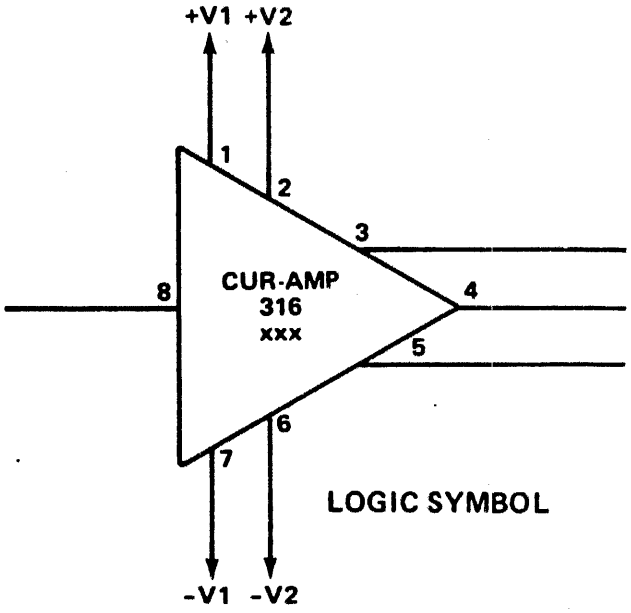
Separate connections are provided for + (V_{CC}) and - (V_{EE}) voltages to both the input and output stages (see electrical schematic diagram). This increases the versatility of operation by allowing a decreased voltage to be applied to the output stage (Q3, Q4), thereby minimizing the power dissipation.

Typical applications: differential input/output op amp, booster amplifier, level shifter, pulse-transformer driver, and transmission-line driver.

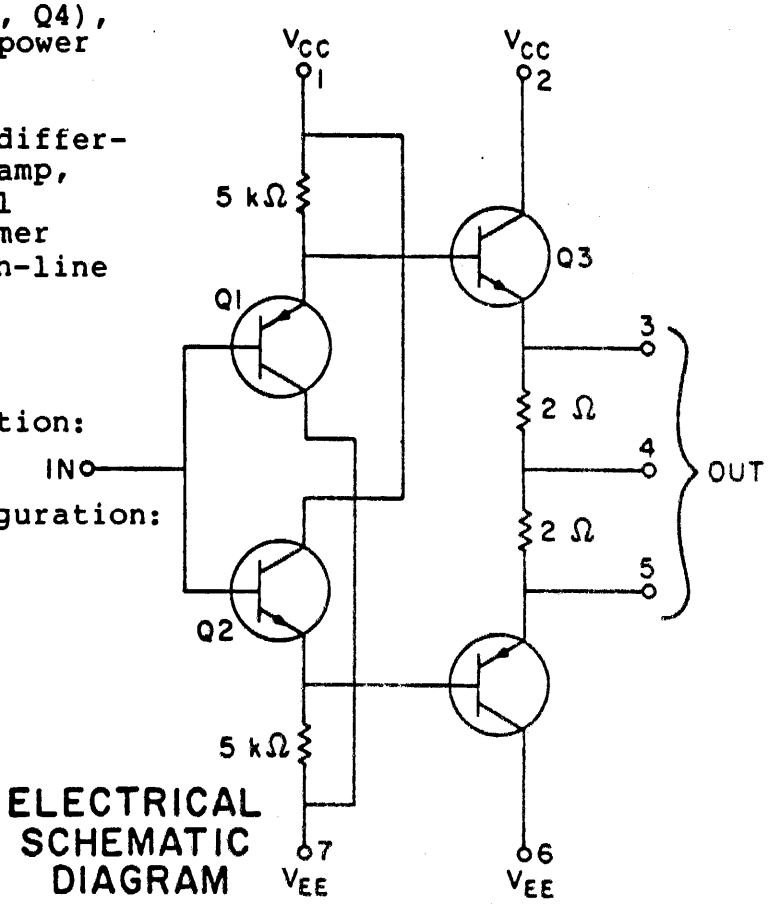
NOTES:

1. Vendor identification: LH0002CH
2. Package pin configuration:





LOGIC SYMBOL



ELECTRICAL SCHEMATIC DIAGRAM

316
Sheet 1 of 1

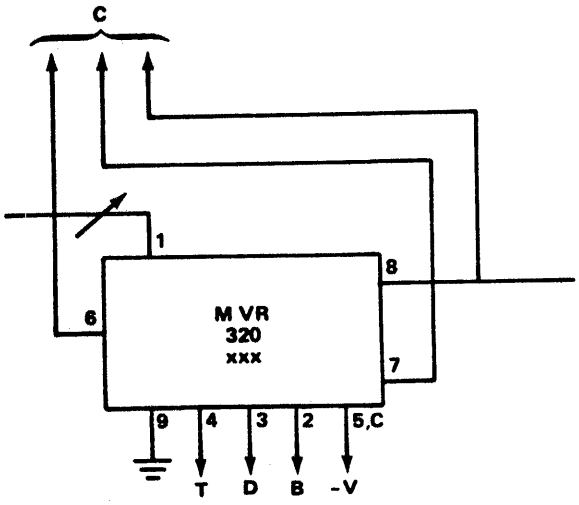
DESCRIPTION

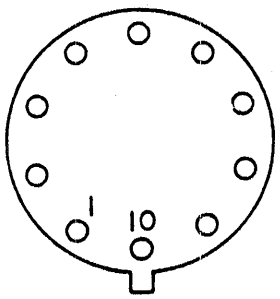
The 320 circuit is a negative voltage regulator that can be programmed by an external resistor to provide any voltage from -40 V to 0 V while operating from a single unregulated supply. Regulation is 1 mV, no load to full load. The full load current of 25 mA can be increased by adding external transistors.

See page 320 Sheets 2 and 3 for typical applications.

NOTES:

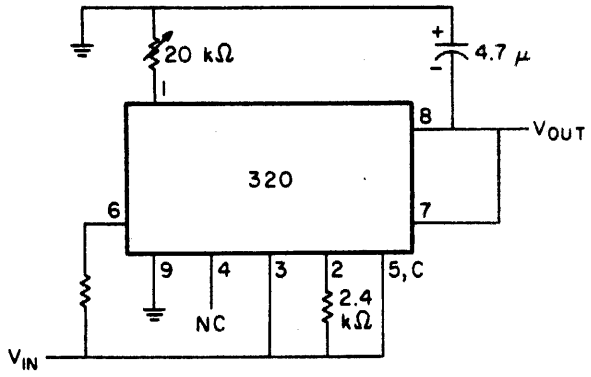
1. Vendor identification: LM304
2. Package pin configuration: (pin 10 is unused)



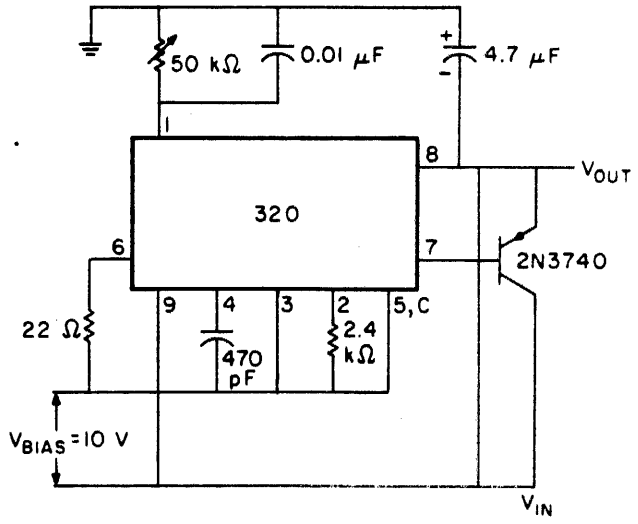


T = TERMINATION
D = DIVIDER COMPONENTS
B = BIAS CIRCUIT (REFERENCE VOLTAGE)
-V = UNREGULATED INPUT
C = CURRENT MONITOR
REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY D
REPLACE m' WITH NOMINAL CURRENT AS DETERMINED BY C

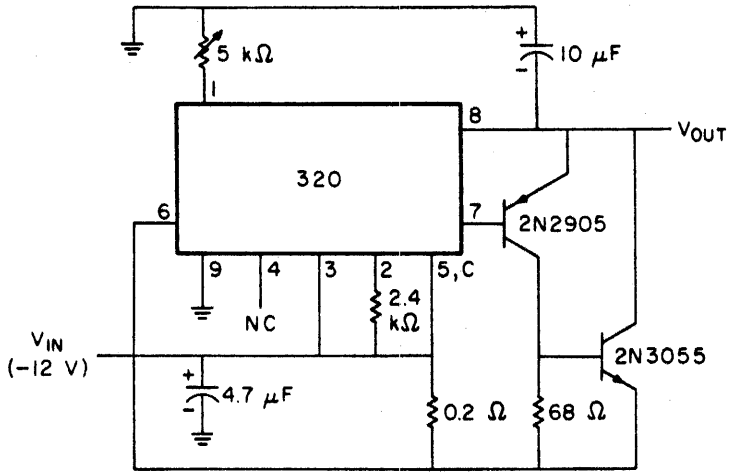
LOGIC SYMBOL



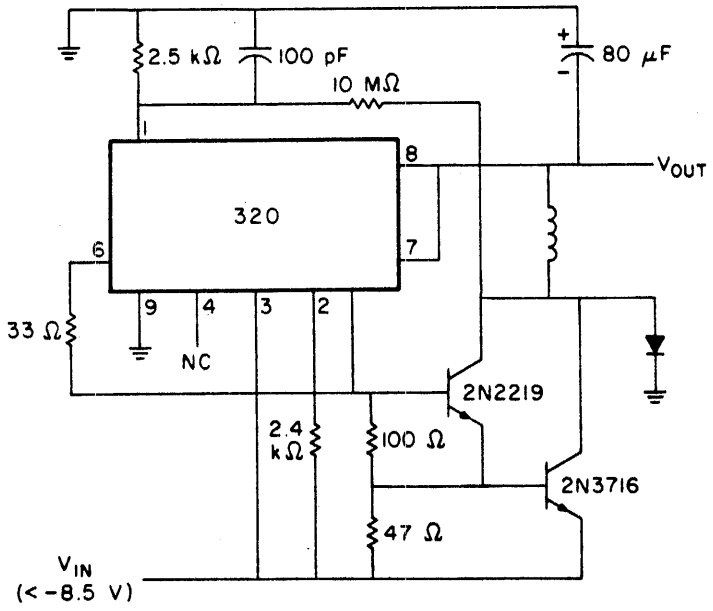
BASIC REGULATOR



SEPARATE BIAS SUPPLY



HIGH-CURRENT REGULATOR



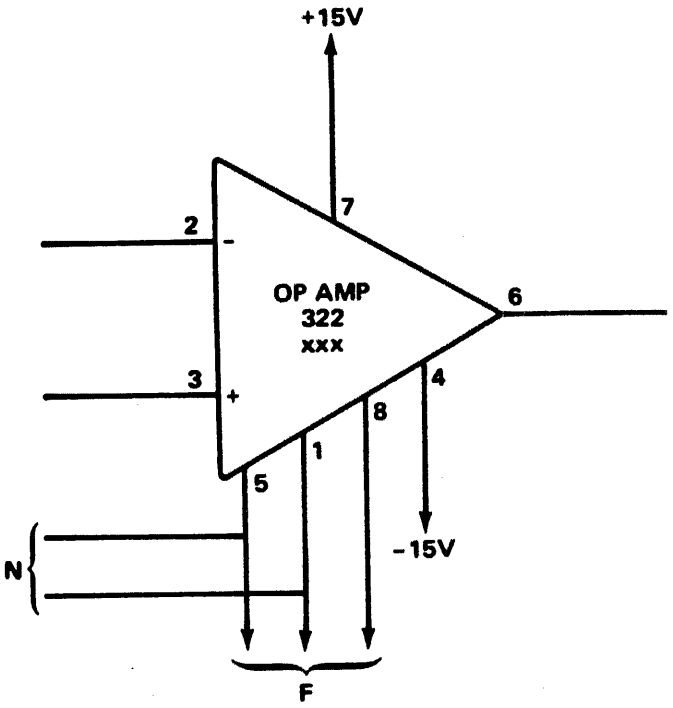
SWITCHING REGULATOR

320
Sheet 3 of 3

DESCRIPTION

Element 322 is a frequency compensated, high-speed operational amplifier.

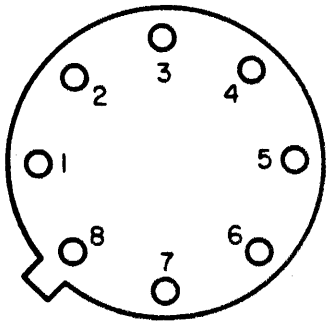
Pin	Function
1	Offset Null/Compensation 1
2	Inverting Input
3	Non-inverting Input
4	-V
5	Offset Null/Compensation 3
6	Output
7	+V
8	Compensation 2



LOGIC SYMBOL

NOTES:

1. Vendor Identification: LM318



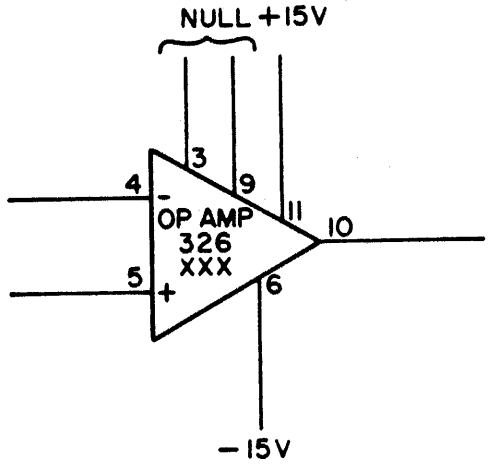
PACKAGE PIN CONFIGURATION

322
Sheet 1 of 1

DESCRIPTION

Element 326 is a high-gain operational amplifier.

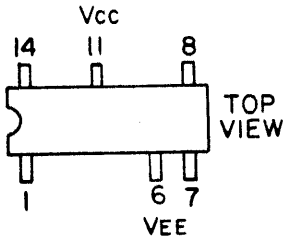
Pin	Function
1	No Contact
2	No Contact
3	Offset Null
4	Inverting Input
5	Non-Inverting Input
6	V-
7	No Contact
8	No Contact
9	Offset Null
10	Output
11	V+
12	No Contact
13	No Contact
14	No Contact



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 741C

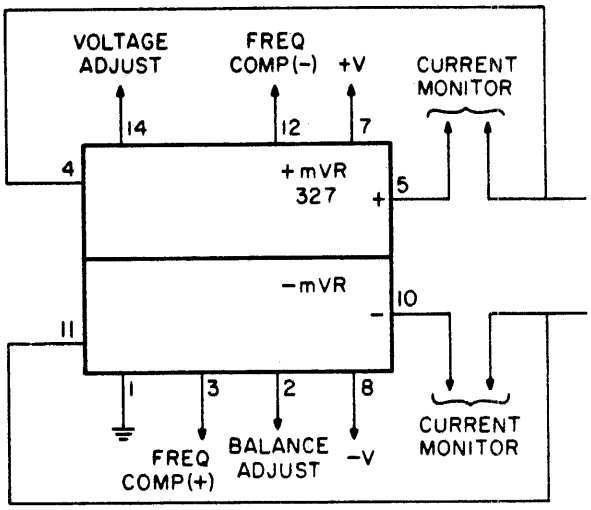


PACKACE PIN CONFIGURATION

DESCRIPTION

Element 327 is a dual-polarity voltage regulator for providing balanced positive and negative output voltages at currents up to 100 mA. Internally, the device is set for ±15 V outputs, but voltage and balance pins permit simultaneous adjustments from 8 to 20 volts. Input voltages up to ±30 V can be used, and current monitor connections provide for adjustable current limiting.

For typical applications, see page 327 Sheets 2 and 3.



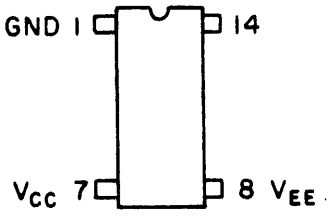
REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY VOLTAGE AND BALANCE ADJUST COMPONENTS.

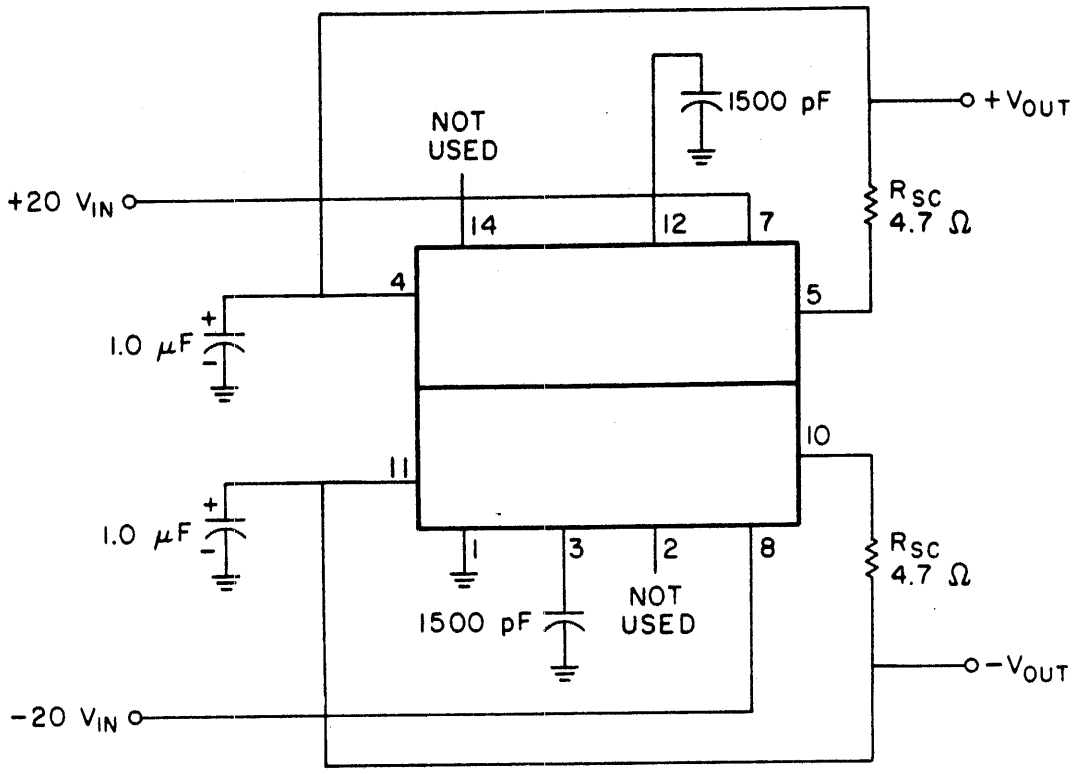
LOGIC SYMBOL

NOTES

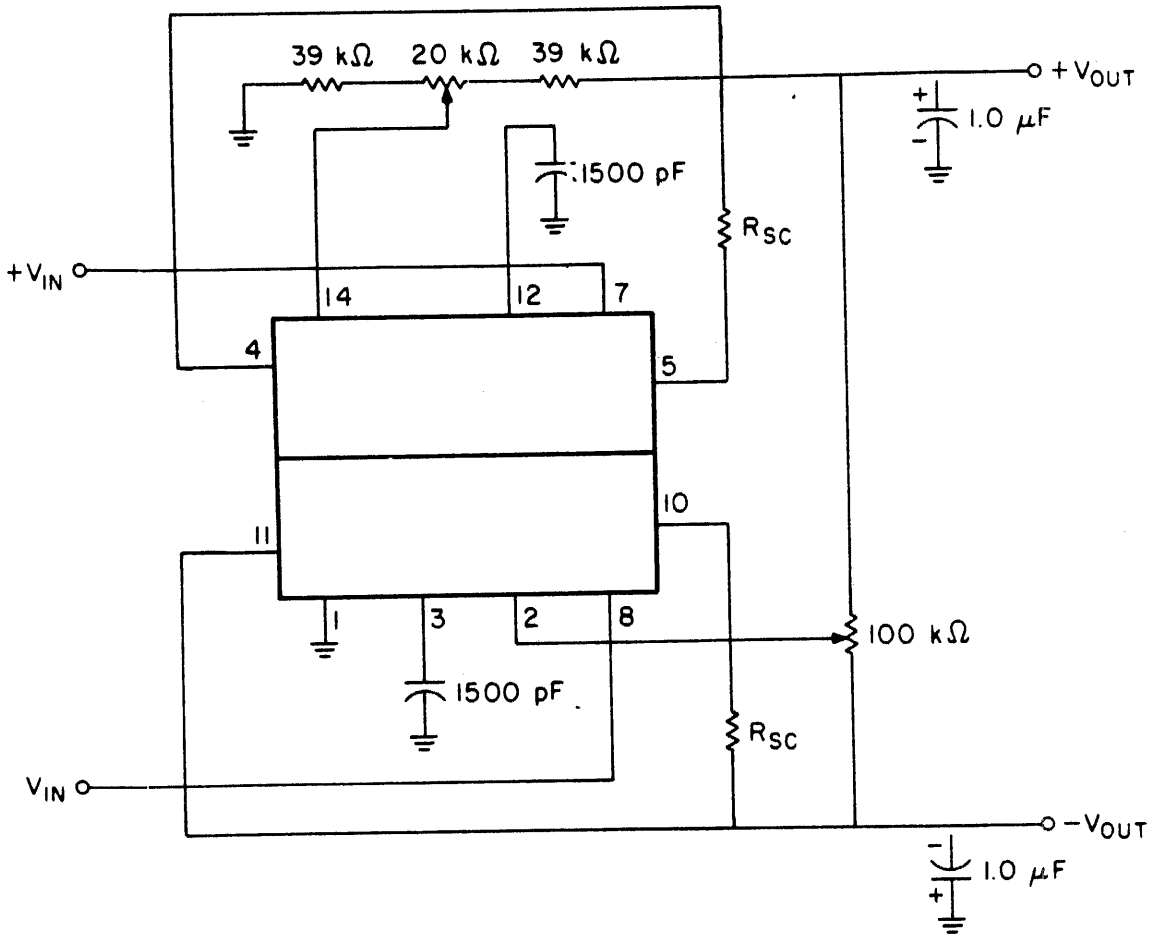
1. Vendor identification: MC1468L

2. Package pin configuration.





BASIC 50 mA REGULATOR



VOLTAGE ADJUST/BALANCE CIRCUIT

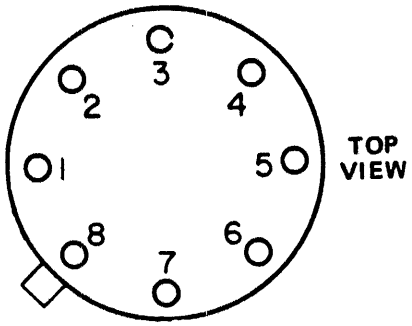
327
Sheet 3 of 3

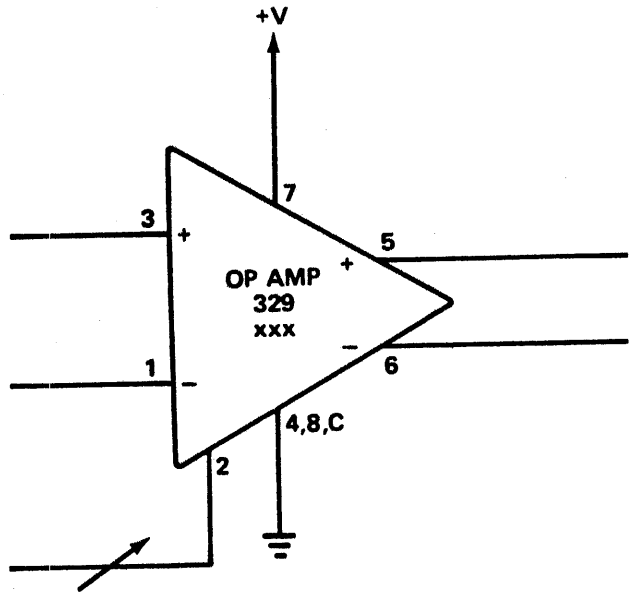
DESCRIPTION

The 329 circuit is a wide-band RF/IF/Audio amplifier with external AGC control.

NOTES:

1. Vendor identification: 1590
2. Package pin configuration. (TO-99 metal case)

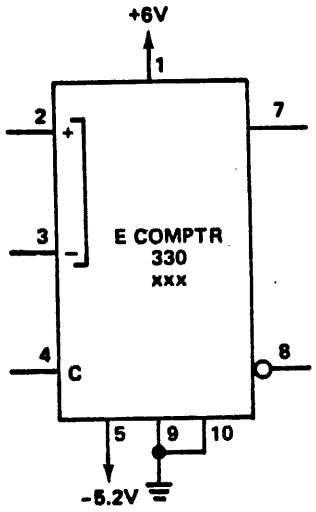




LOGIC SYMBOL

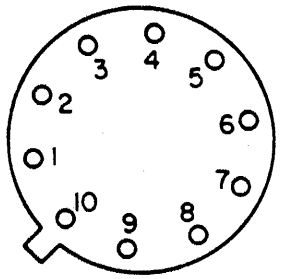
DESCRIPTION

The 330 circuit is a differential voltage comparator. The circuit has differential analog inputs and complementary logic outputs compatible with ECL. A latch function allows the comparator to be used in a sample-hold mode. If the latch enable input is high, the comparator functions normally. When the latch enable goes low, the comparator outputs are locked in their existing logical states.



LOGIC SYMBOL

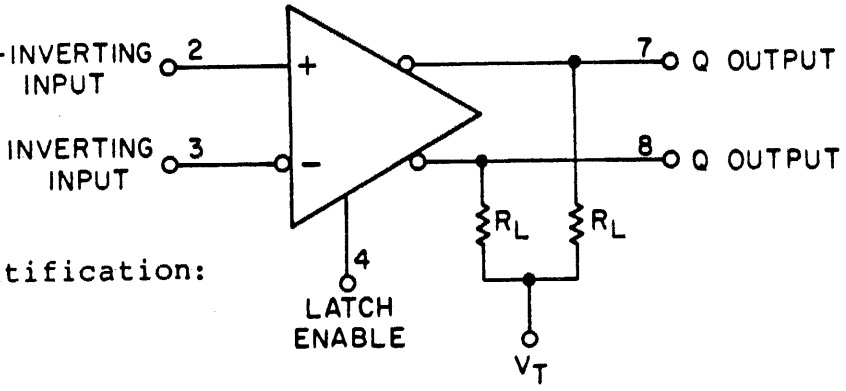
Pin	Function
1	+V
2	Non-inverting Input
3	Inverting Input
4	Latch Enable
5	-V
6	No Connection
7	Q Output
8	$\bar{Q}$ Output
9	GND
10	GND



PACKAGE PIN CONFIGURATION

NOTE:

1. Vendor Identification: AM685



FUNCTION DIAGRAM

330
Sheet 1 of 1

DESCRIPTION

Element 331A is a dual-polarity tracking voltage regulator that provides balanced or unbalanced positive and negative output voltages at currents up to 200 mA. A single external resistor adjustment changes both outputs between the limits of ±50 mV and ±42 V. The 331A comes in a 9-pin (type H) "top hat" package that can dissipate up to 3 W. Both output voltages drop to zero if the junction temperature rises above 175°C.

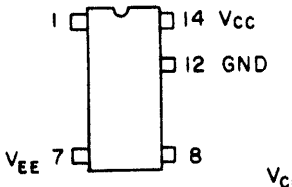
Element 331 is similar to the 331 A, except that it comes in a 14-pin DIP that can dissipate up to 900 mW.

NOTES:

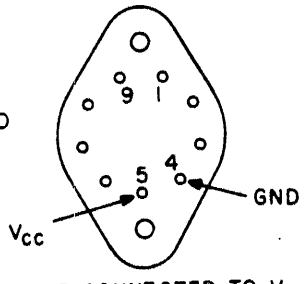
1. Vendor identification:

Element	Vendor Number
331	RC4194D
331A	RC4194TK

2. Package pin configuration.



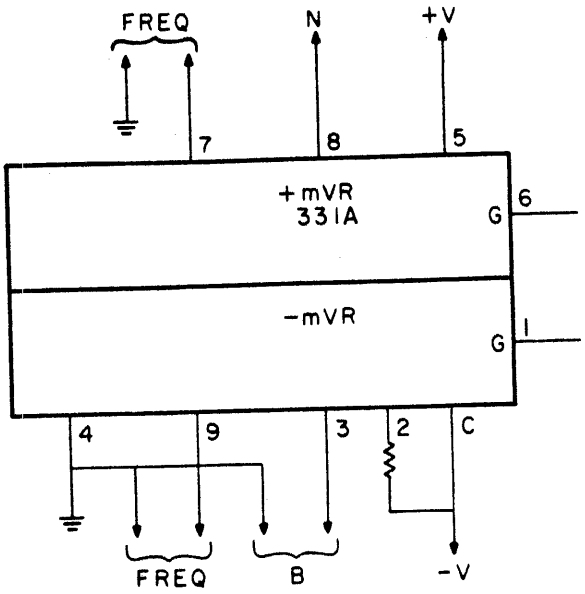
331



CASE CONNECTED TO V_{EE}

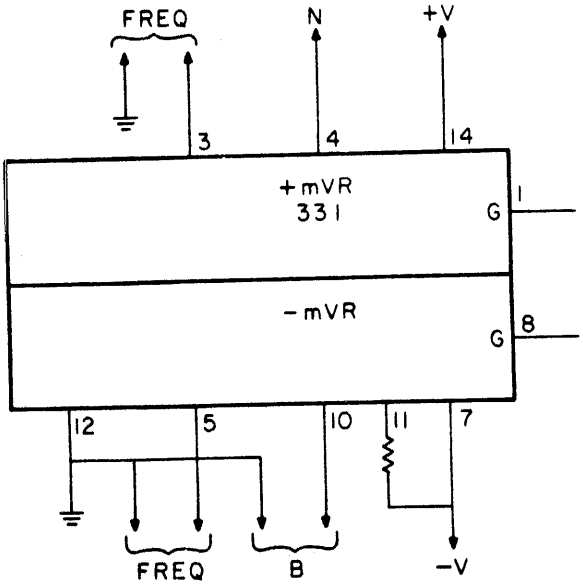
331A

331A



OR

331



REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY BIAS (B) AND BALANCE (N) COMPONENTS

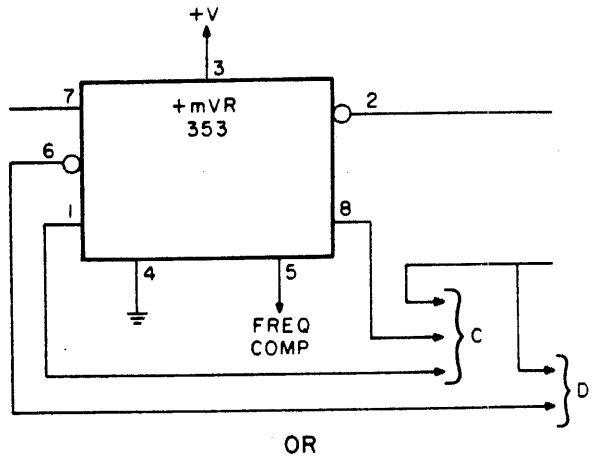
LOGIC SYMBOL

331
Sheet 1 of 1

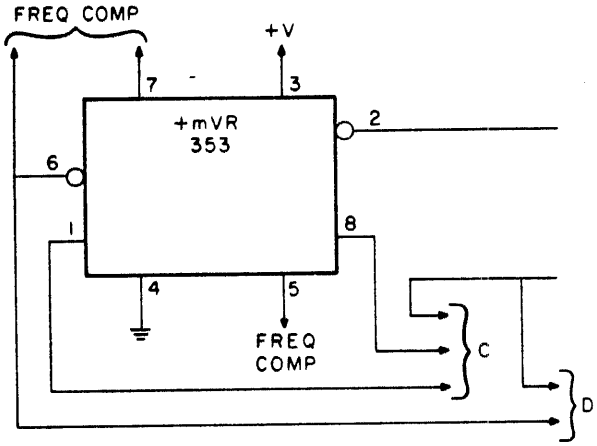
DESCRIPTION

The 332 and 353 circuits are positive voltage regulators. Output voltage is adjustable from 4.5 to 40 volts. The full-load output current of the 332 is 45 mA, that of the 353 is 25 mA. Either of these may be increased in excess of 10 A by using an external pass transistor.

The 332 comes in a 8-pin metal can and the 353 in an 8-pin DIP.



OR

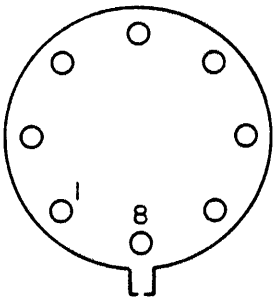


NOTES:

1. Vendor identification:

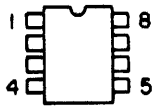
Element	Vendor Number
332	LM305A
353	LM376

2. Package pin configuration:



PIN 4 CONNECTED TO CASE

332



353

DESCRIPTION

Element 333 is a dual-polarity tracking voltage regulator that provides balanced positive and negative 15 V outputs at currents up to 100 mA. The type-H packaging permits heat dissipation of up to 2.4 W. Both output voltages drop to zero if the junction temperature rises above 175°C.

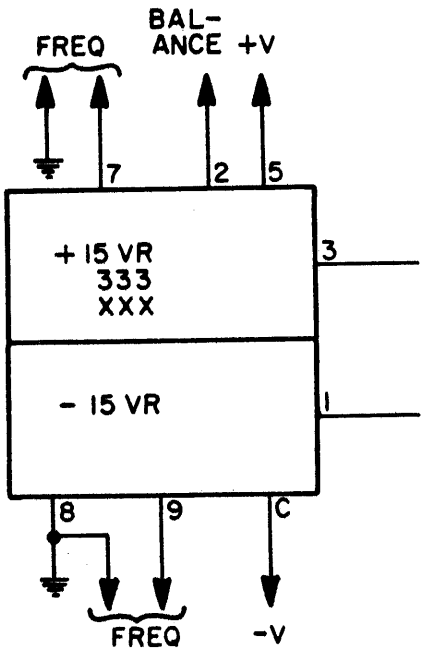
The 333 circuit may also be used as a single-output regulator with up to +50 V output, where:

(V out +3 V) |V in |60 V

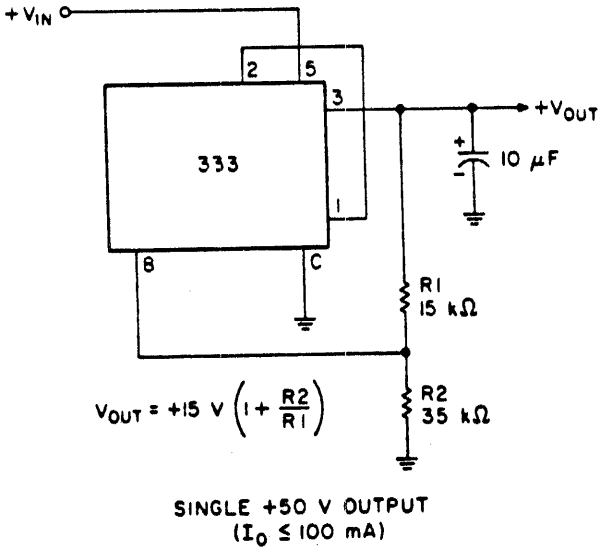
NOTES

1. Vendor identification RC4195TK

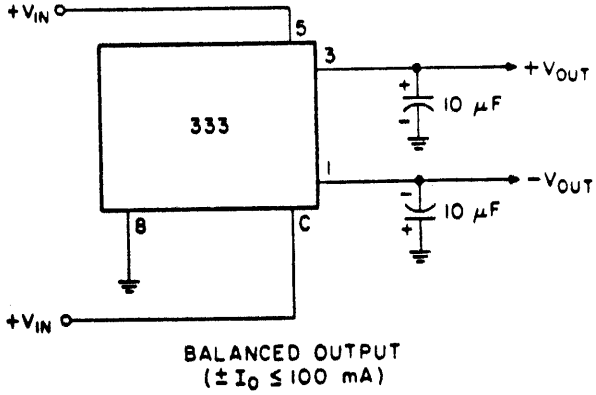
2. Package pin configuration:



LOGIC SYMBOL



SINGLE +50 V OUTPUT
($I_O \leq 100$ mA)



BALANCED OUTPUT
($\pm I_O \leq 100$ mA)

TYPICAL APPLICATIONS

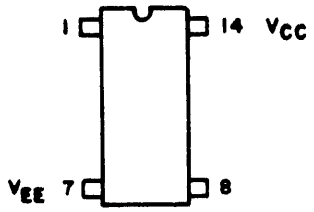
333
Sheet 1 of 1

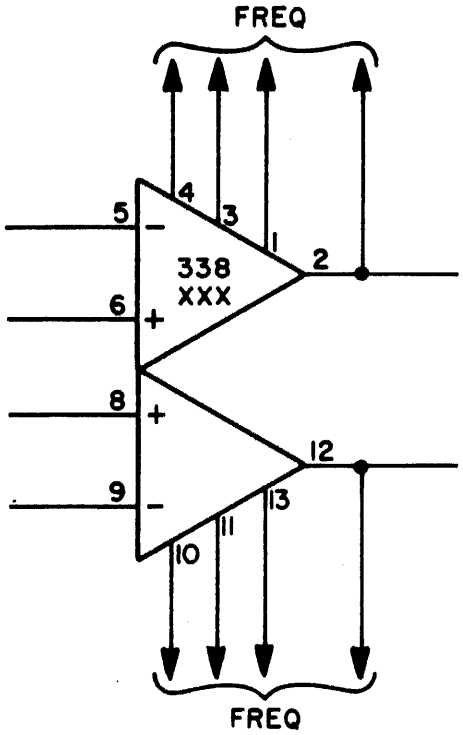
DESCRIPTION

Element 338 is a dual high-gain operational amplifier.

NOTES:

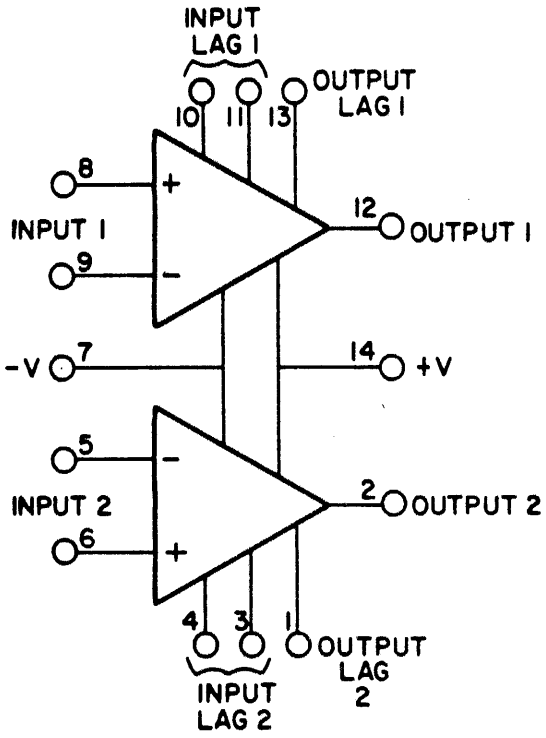
1. Symbol sections may appear separately.
2. Vendor identification: MC1437
3. Package pin configuration:





LOGIC SYMBOL

EQUIVALENT CIRCUIT



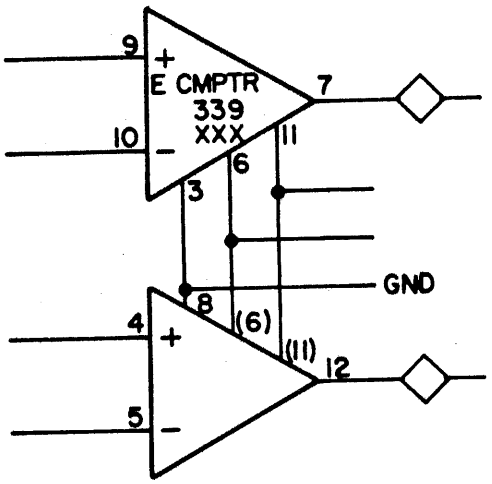
338
Sheet 1 of 1

DESCRIPTION

Element 339 consists of two high-speed voltage comparators in one package. Each section provides an open-collector output capable of driving lamps or relays requiring up to 25 mA. Inputs and outputs can be isolated from system ground.

The 339 can operate from a single +5 V supply, or from ± supplies with a total potential difference of up to 36 V. Maximum differential input voltage is ±5 V.

If pin 4 (9) is more positive than pin 5 (10), the output is open. If pin 4 (9) is equal to or less positive than pin 5 (10), the output is grounded.



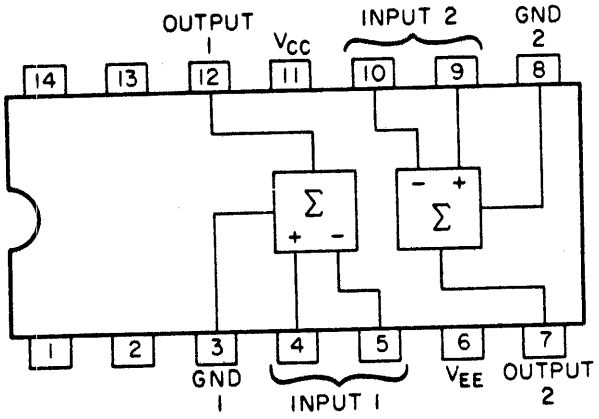
LOGIC SYMBOL

NOTES

1. If sections appear separately, the supply-voltage pins are repeated as needed and only the applicable ground pin is shown for each section.

2. Vendor identification: LM319

3. Package pin configuration and functional diagram.

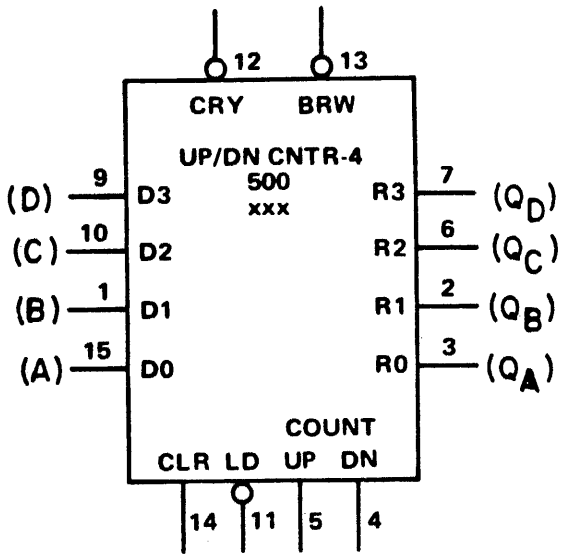


339

DESCRIPTION

The 500 circuit is a synchronous 4-bit up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable; that is, the counter may be preset to any state by entering the desired data at the data inputs while the load input (pin 11) is low. The output will then change to agree with the data inputs independently of the count pulses. A high level applied to the clear input forces all outputs to the low level. The clear function is independent of the count and load inputs.



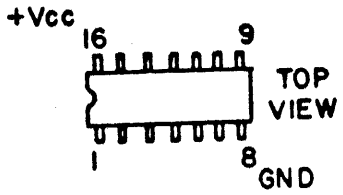
LOGIC SYMBOL

NOTES:

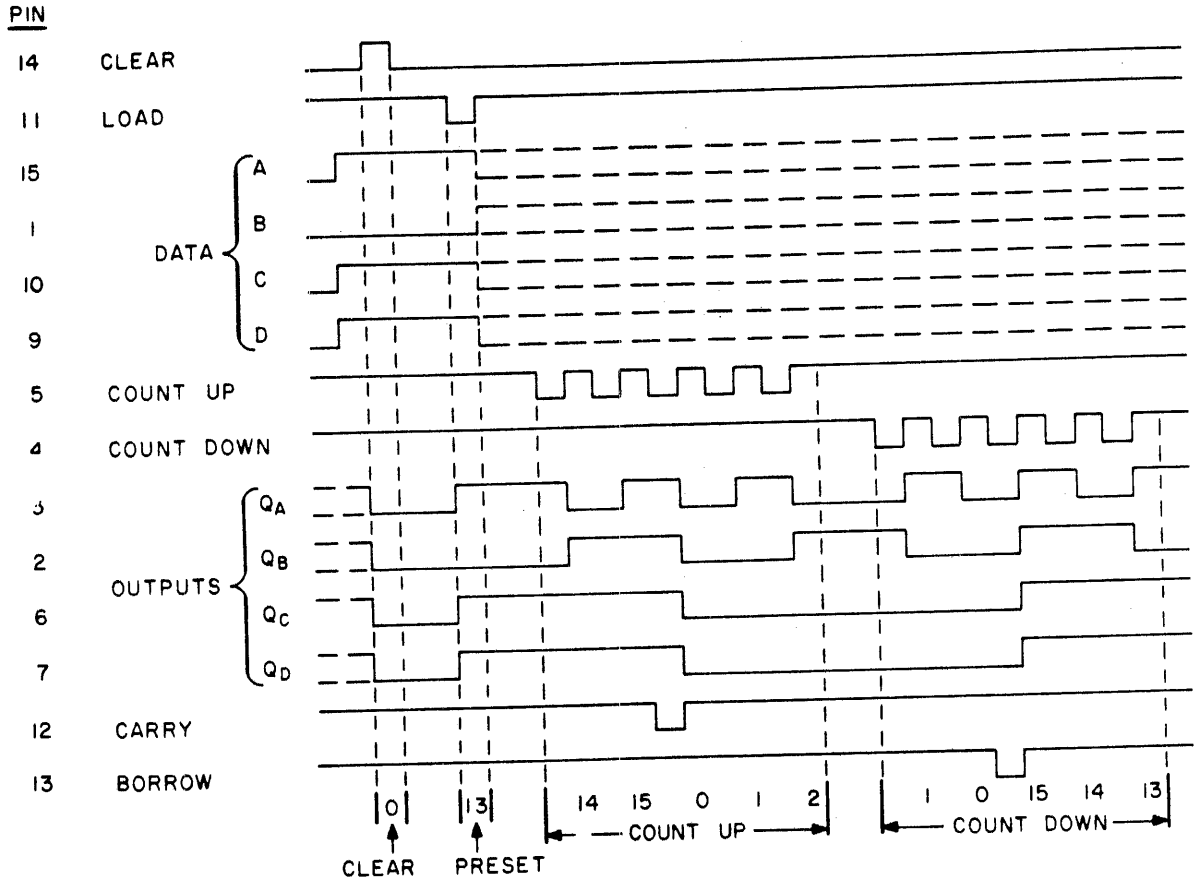
1. Input/Output identifiers are not part of the symbol.

2. Vendor identification:

Element	Vendor Number
500	74193, 9366
500LS	74LS193

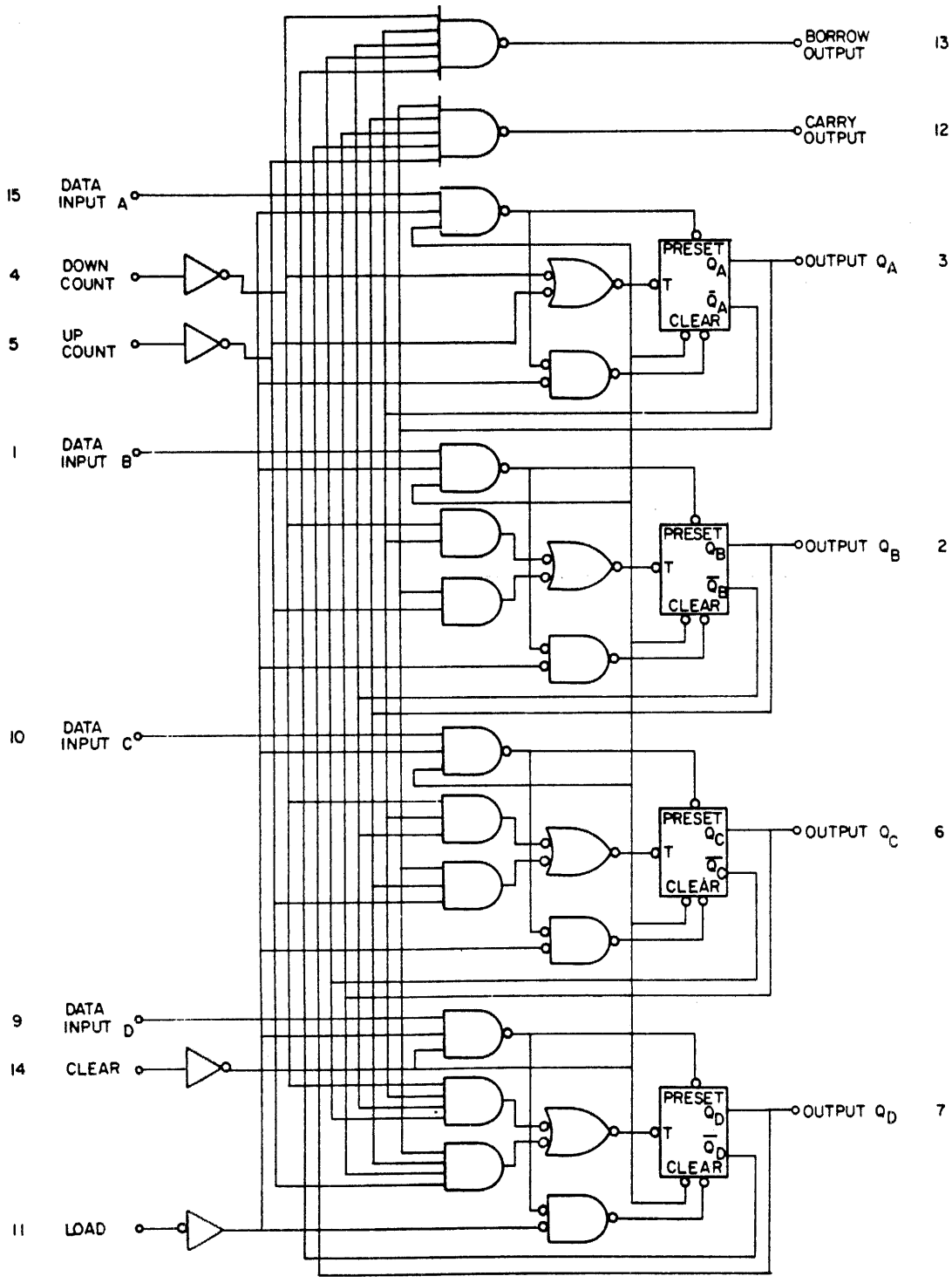


3. Package pin configuration.



NOTE:
ILLUSTRATED ABOVE IS THE FOLLOWING SEQUENCE:
1. CLEAR OUTPUTS TO ZERO.
2. LOAD (PRESET) TO BCD THIRTEEN.
3. COUNT UP TO FOURTEEN, FIFTEEN, CARRY, ZERO, ONE AND TWO.
4. COUNT DOWN TO ONE, ZERO, BORROW, FIFTEEN, FOURTEEN AND THIRTEEN.

COUNTING SEQUENCE

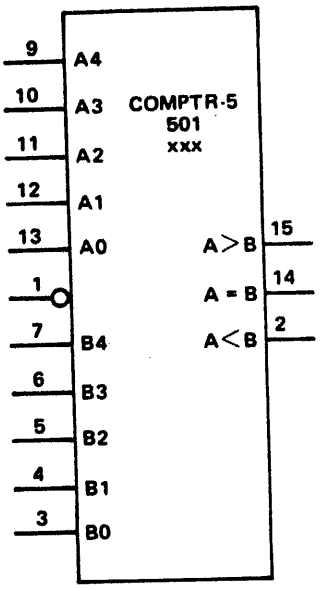


FUNCTION DIAGRAM

500
Sheet 3 of 3

DESCRIPTION

The 501 circuit is a 5-bit comparator that provides comparison between two 5-bit words and gives three outputs: "less than", "greater than", and "equal to". A high level on the active low enable (pin 1) forces all three outputs low.

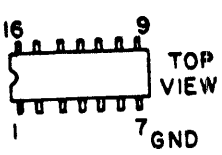


LOGIC SYMBOL

NOTES:

1. Vendor identification: 9324

2. Pin names:



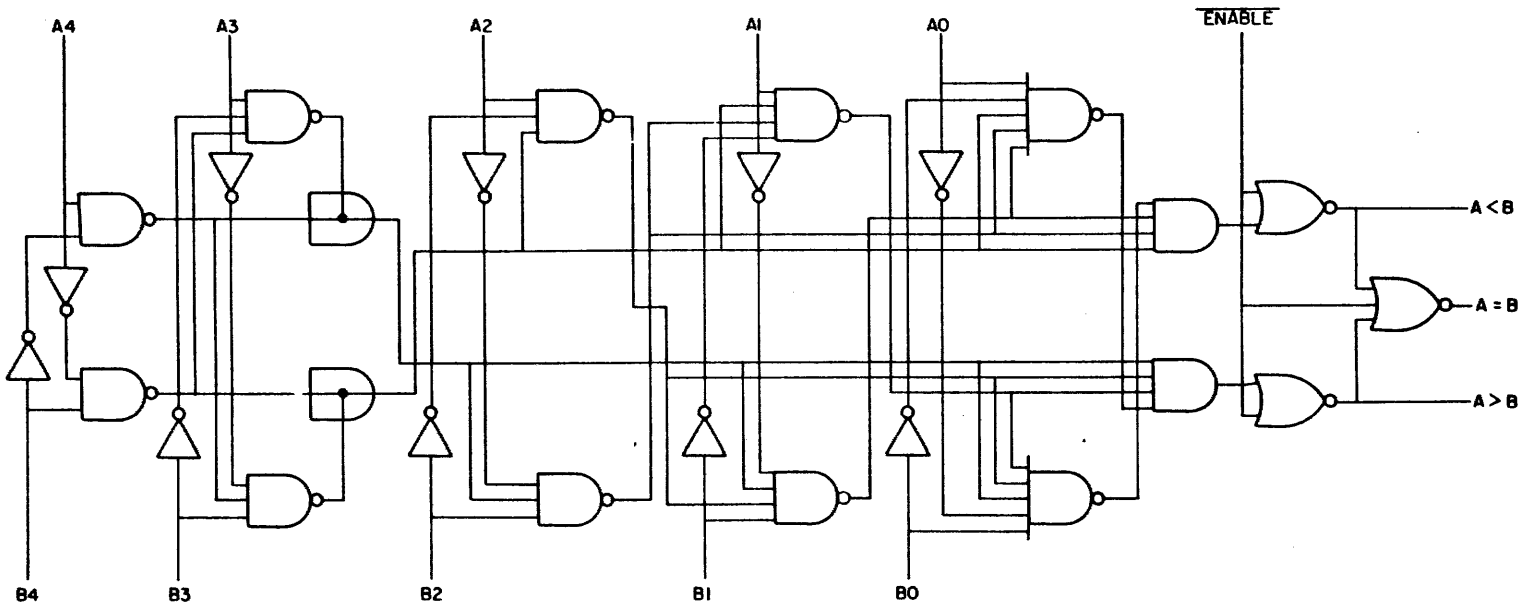
Pin	Function
1	Enable (active low) input
9,10,11, 12,13	Word A parallel inputs
3,4,5, 6,7	Word B parallel inputs
2	A Less Than B (A<B) output
14	A Equal to B (A=B) output
15	A Greater Than B (A>B) output

3. Package pin configuration

	INPUT		OUTPUT		
I	A	B	A<B	A>B	A=B
H	X		L	L	L
L	WORD A = WORD B		L	L	H
L	WORD A > WORD B		L	H	L
L	WORD A < WORD B		H	L	L

H = HIGH LEVEL
L = LOW LEVEL
X = EITHER HIGH OR LOW LEVEL

TRUTH TABLE

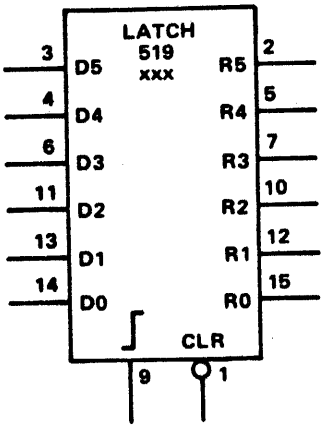


FUNCTION DIAGRAM

501
Sheet 2 of 2

DESCRIPTION

The 519 circuit is a register made up of six D-type flip-- flops with common clock and clear inputs.



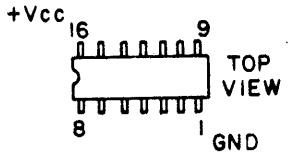
LOGIC SYMBOL

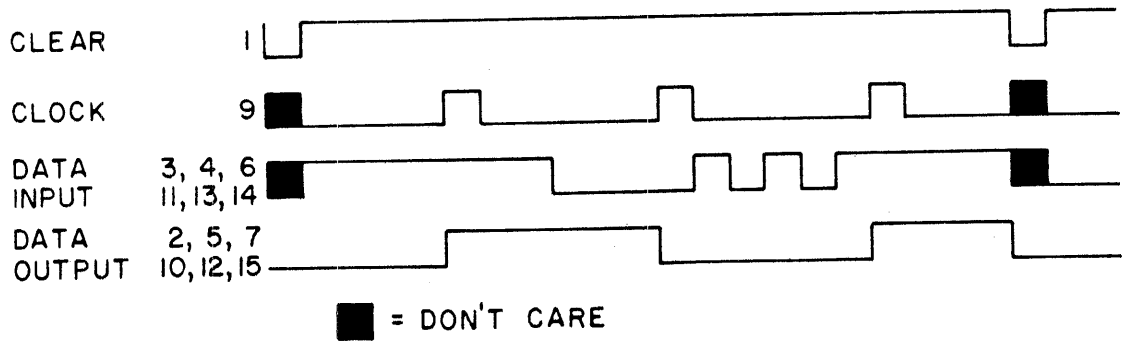
NOTES:

1. Vendor identification:

Element	Vendor Number
519	74174
519S	74S174

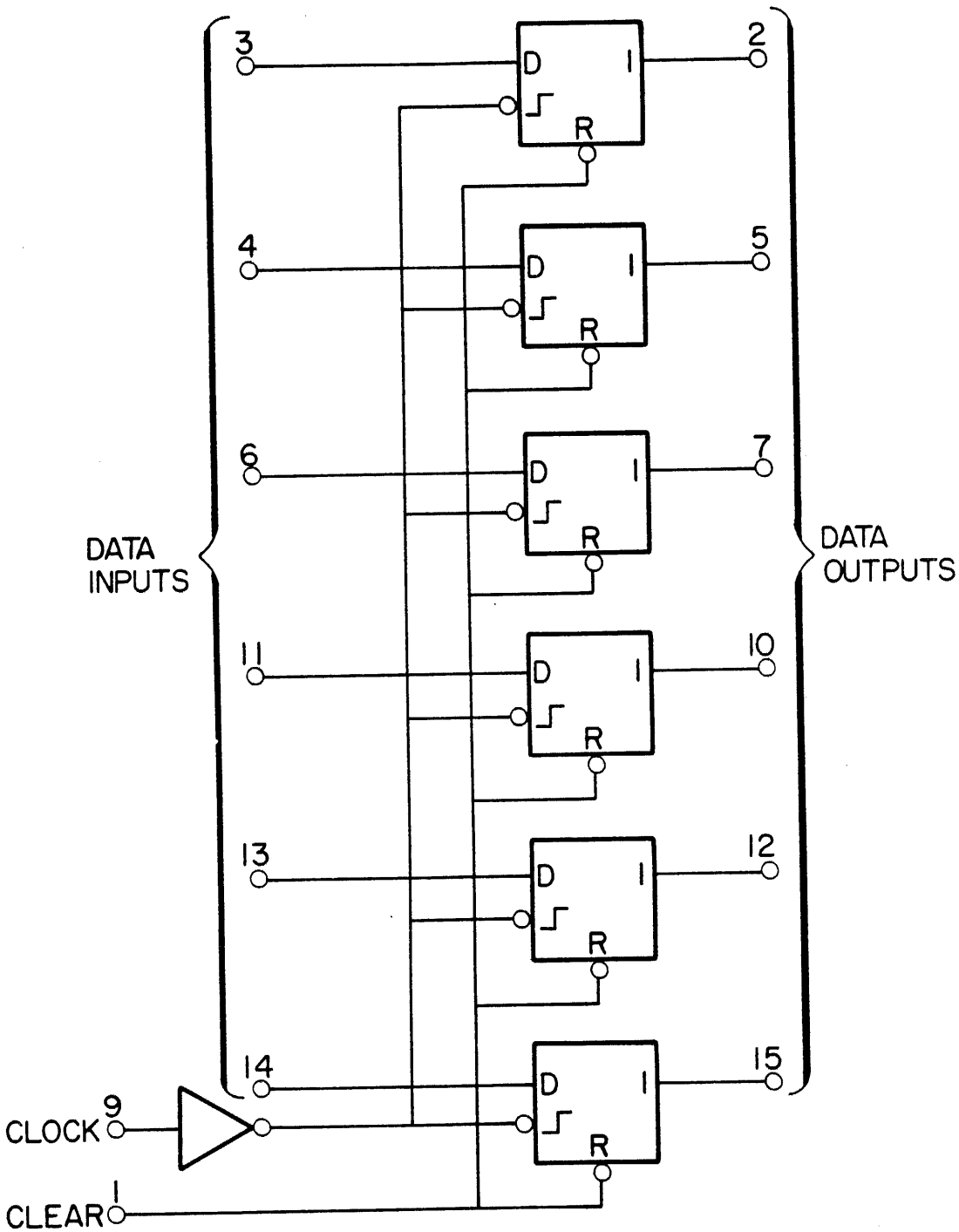
2. Package pin configuration.





FUNCTION SEQUENCE

519
Sheet 1 of 2

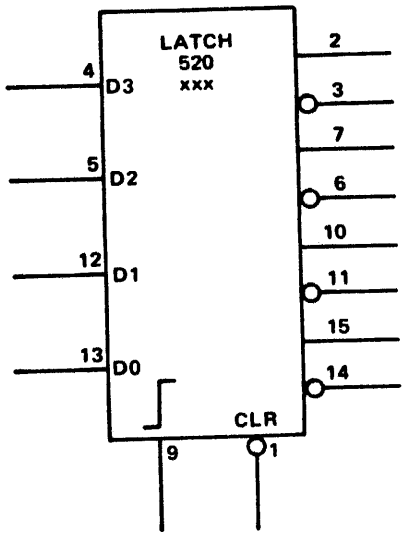


FUNCTION DIAGRAM

519
Sheet 2 of 2

DESCRIPTION

Element 520 contains four positive-edge-triggered D-type flip-flops with common clock and reset (clear) inputs. Each FF has complementary outputs. Information at the input is transferred to the output on the positive-going transition of the clock pulse. When the clock is either high or low, input data has no effect on the outputs.



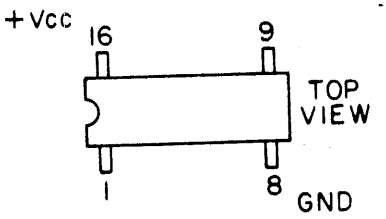
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
520	74175
520LS	74LS175
520S	74S175

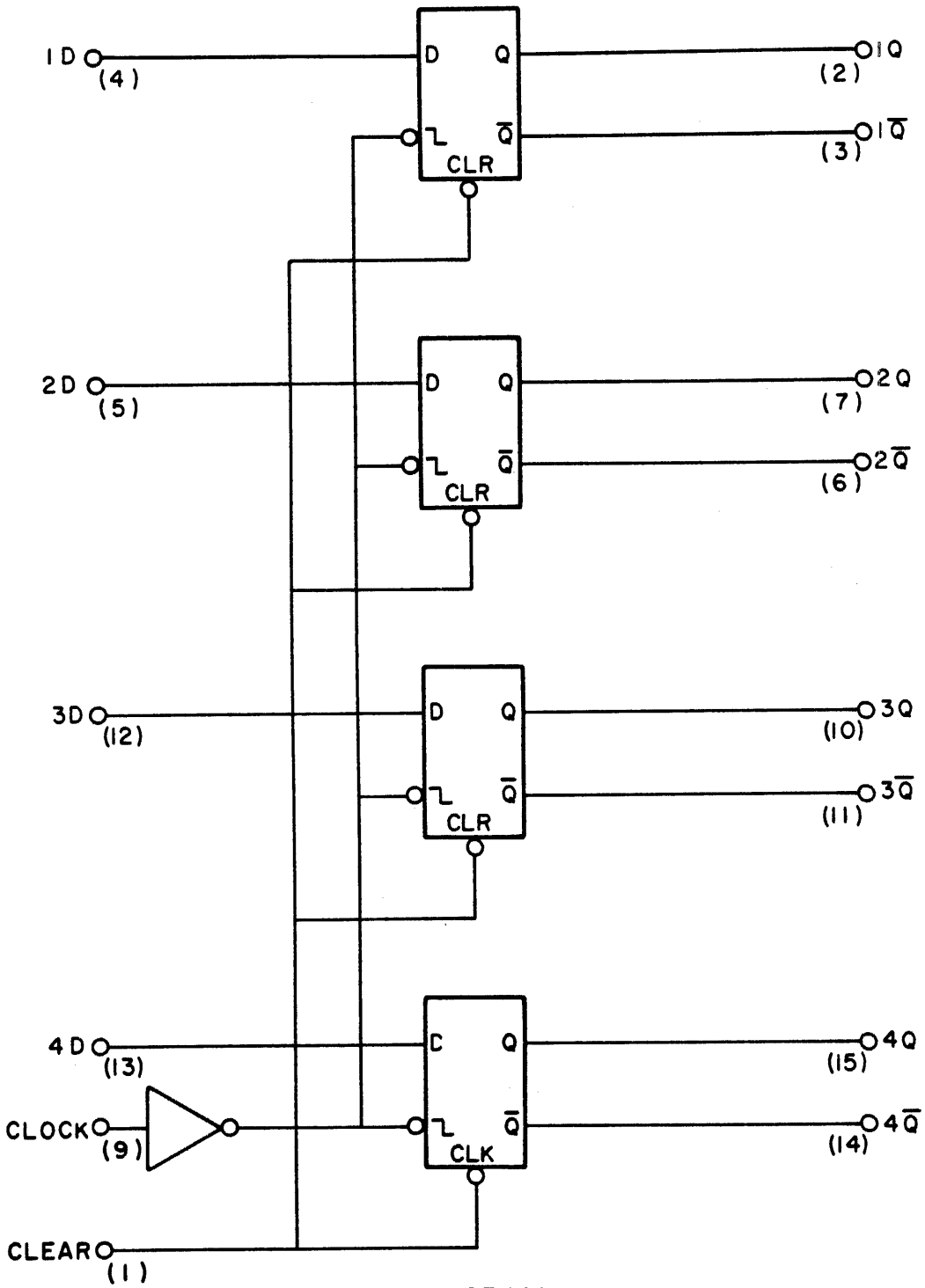
2. Package pin configuration.



INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	NC	NC

↑ = TRANSITION FROM LOW TO HIGH LEVEL
X = DON'T CARE
NC = SAME AS BEFORE INDICATED INPUT CONDITIONS WERE ESTABLISHED

TRUTH TABLE



FUNCTION DIAGRAM

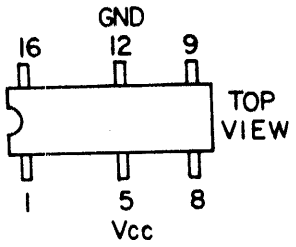
520
Sheet 2 of 2

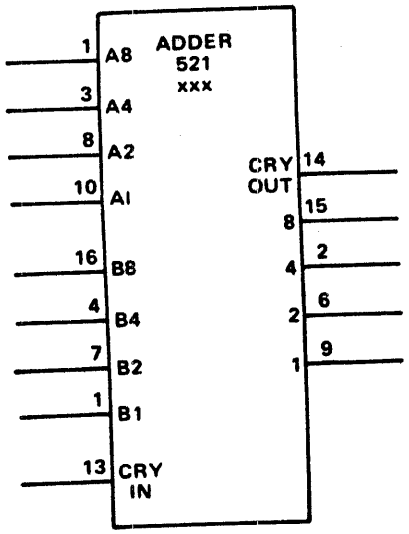
DESCRIPTION

The 521 circuit performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit.

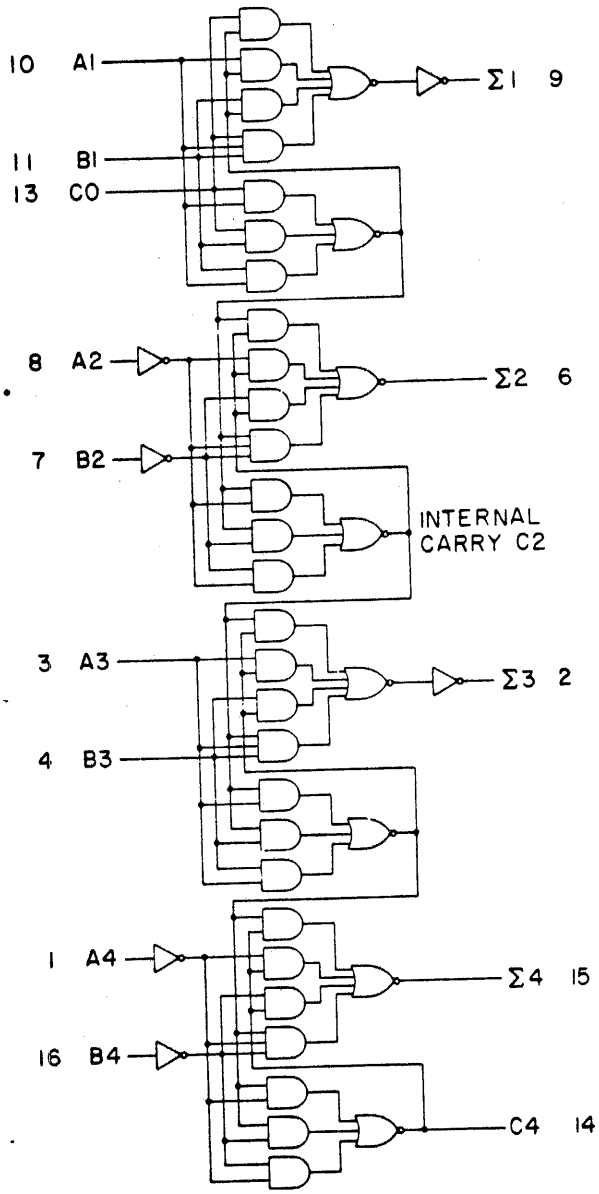
NOTES:

1. Vendor identification: 7483
2. Package pin configuration.





LOGIC SYMBOL



FUNCTION DIAGRAM

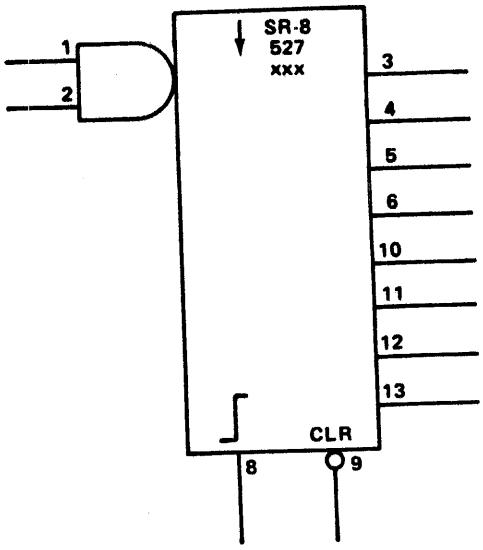
INPUT				OUTPUT					
				WHEN CO=L			WHEN CO=H		
						WHEN C2=L			WHEN C2=H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	L	H	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE 1: INPUT CONDITIONS AT A1, A2, B1, B2, AND CO ARE USED TO DETERMINE OUTPUTS Σ1 AND Σ2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4, ARE THEN USED TO DETERMINE OUTPUTS Σ3, Σ4, AND C4.

TRUTH TABLE

DESCRIPTION

The 527 circuit is an 8-bit shift register with gated serial inputs and an asynchronous clear. The gated serial inputs (pins 1 and 2) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

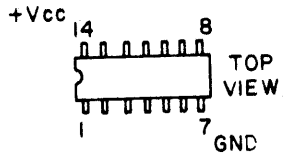


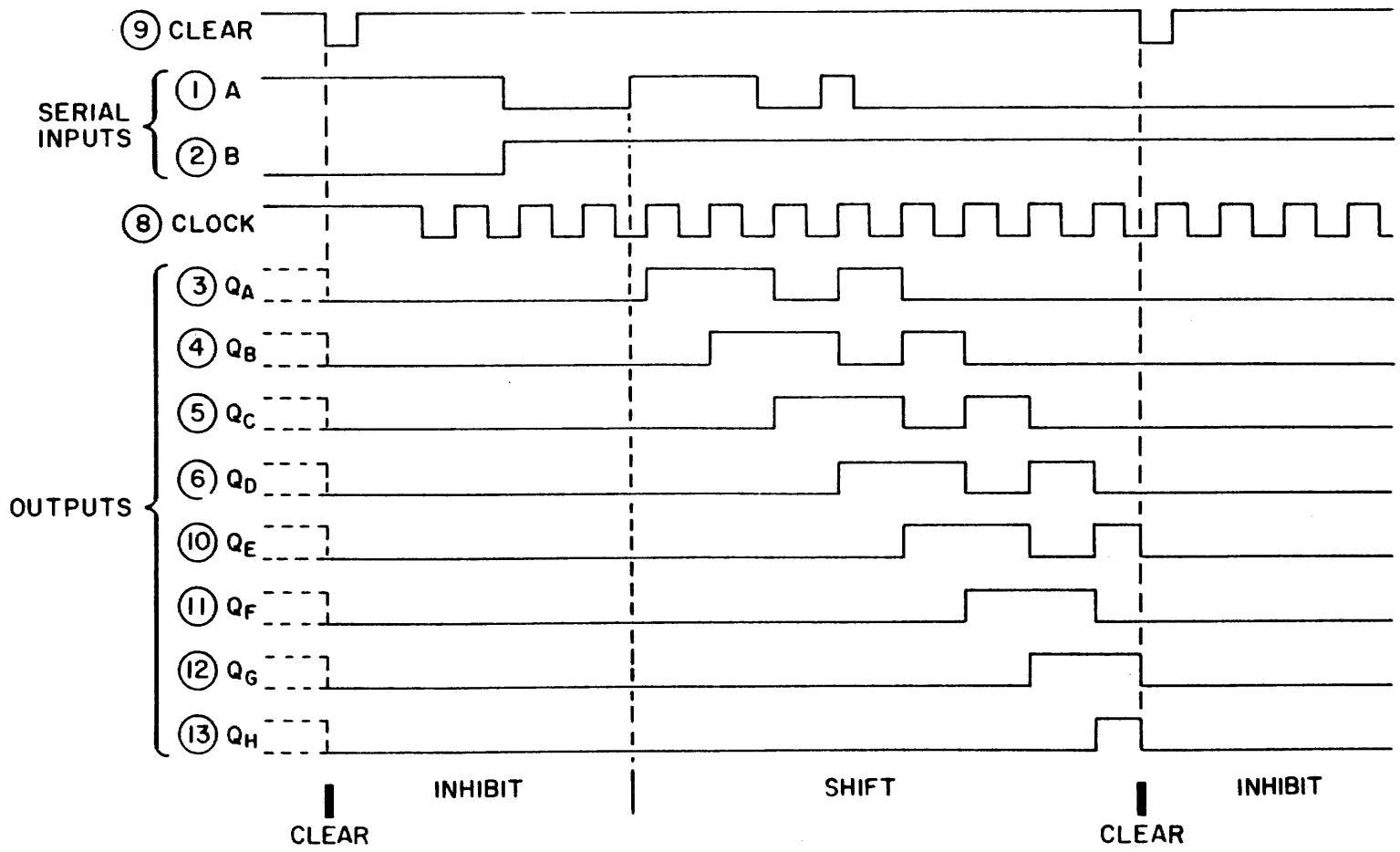
LOGIC SYMBOL

NOTES:

1. Vendor identification: 74164, 8570

2. Package pin configuration.

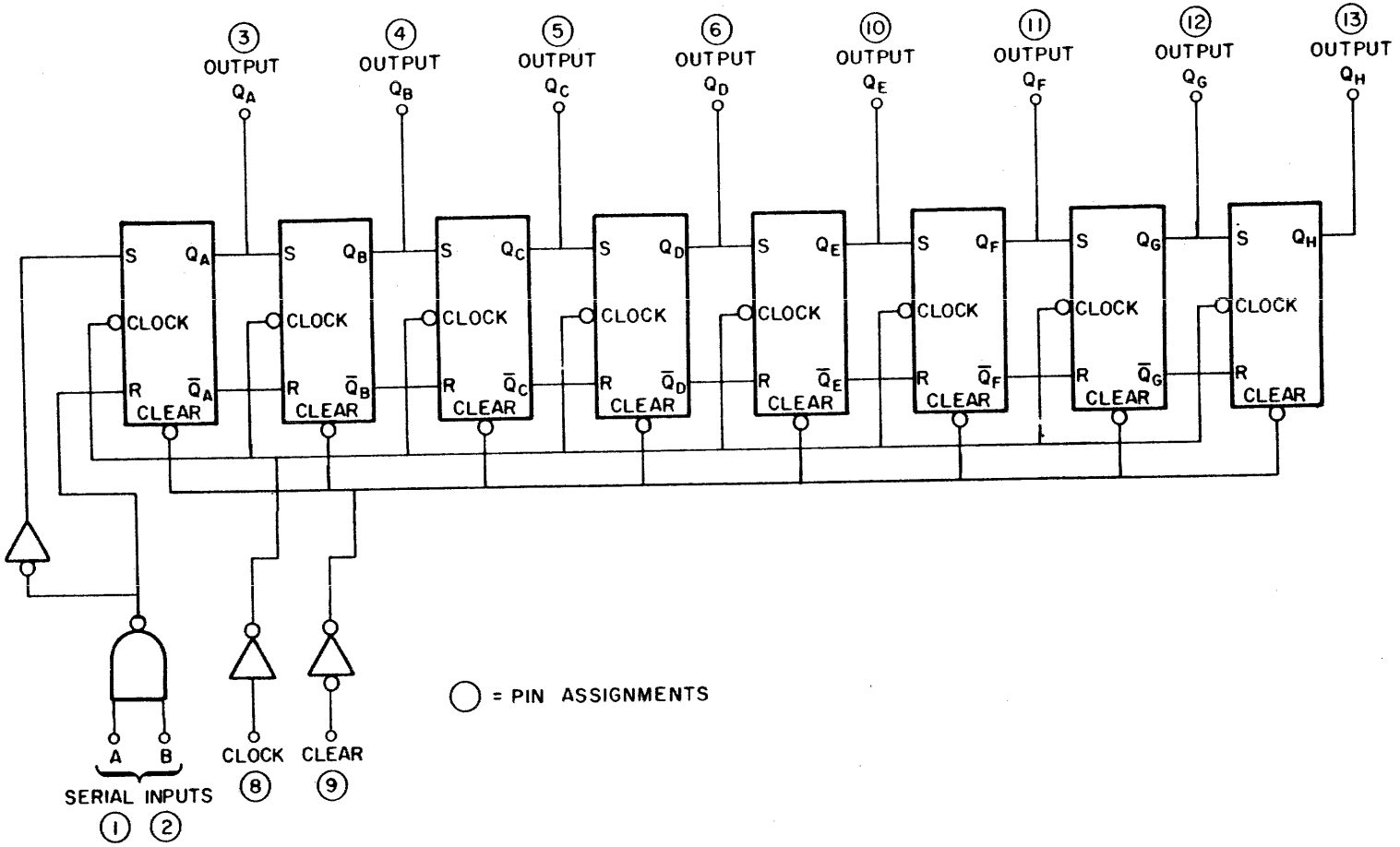




NOTES: 1. TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES.
2. ◯ = PIN ASSIGNMENTS.

FUNCTION SEQUENCE

527
Sheet 2 of 3



FUNCTION DIAGRAM

527
Sheet 3 of 3

DESCRIPTION

Element 538 is a dual 1-of-4 decoder with low-active outputs.

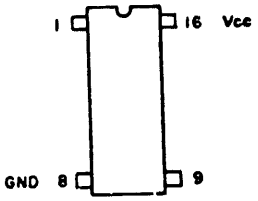
NOTES:

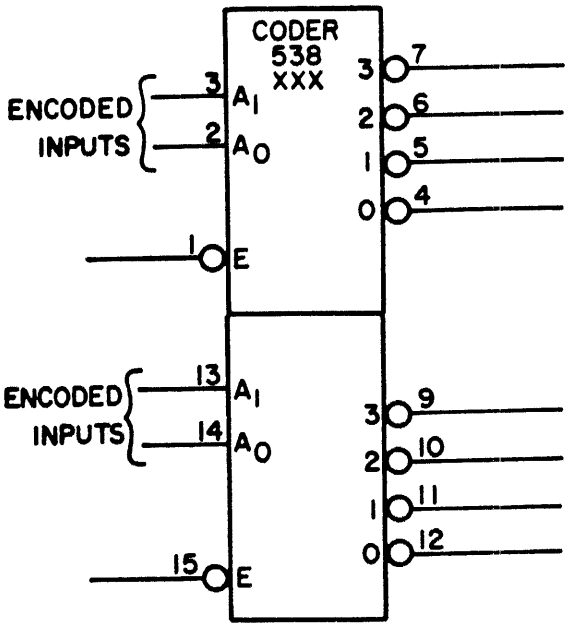
1. Symbol sections may appear separately.

2. Vendor identification:

Element	Vendor Number
538	9321
538S	74S139
538LS	74LS139

3. Package pin configuration.





LOGIC SYMBOL

INPUTS			OUTPUTS			
INH/ ENA	1	2	0	1	2	3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

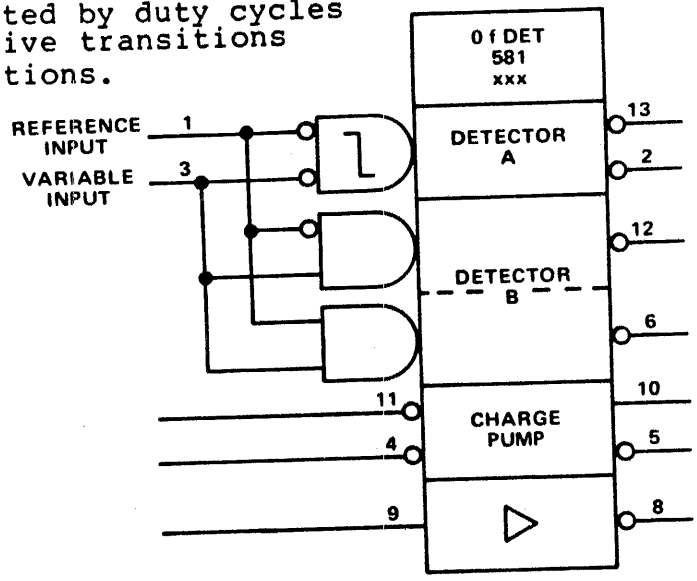
TRUTH TABLE

538
Sheet 1 of 1

DESCRIPTION

The 581 circuit is a phase-frequency detector. This device contains two digital phase detectors, an emitter following amplifier, and a charge pump circuit that converts TTL inputs to a dc voltage for use in frequency discrimination and phase-locked-loop applications.

The two phase detectors have common inputs. Phase-frequency detector A is locked in (indicated by both outputs high) when the negative transitions of the variable input (pin 3) and the reference input (pin 1) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, output pin 13 goes low; conversely, output pin 2 goes low when the variable input is higher in frequency or leads the reference input in phase. The variable and reference inputs to phase detector A are not affected by duty cycles because negative transitions control operations.



LOGIC SYMBOL

581
Sheet 1 of 2

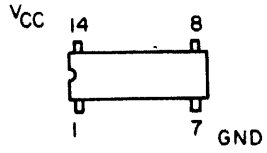
Phase detector B is locked in when the variable input phase lags the reference phase by 90° (indicated by output pins 6 and 12 alternately going low with equal pulse widths). If the variable input lags by more than 90°, pin 12 will remain low longer than pin 6. Conversely, if the variable input phase lags the reference phase by less than 90°, pin 6 remains low longer. In phase detector B, the variable input and the reference input must have 50% duty cycles.

The charge pump accepts the phase detector outputs and converts them to fixed-amplitude positive and negative pulses.

NOTES:

1. Vendor identification: 4044, 4344

2. Package pin configuration



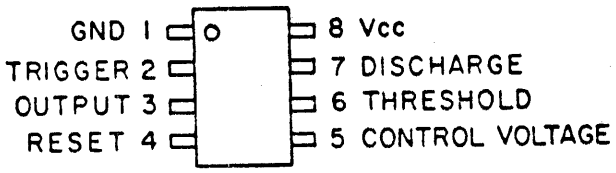
DESCRIPTION

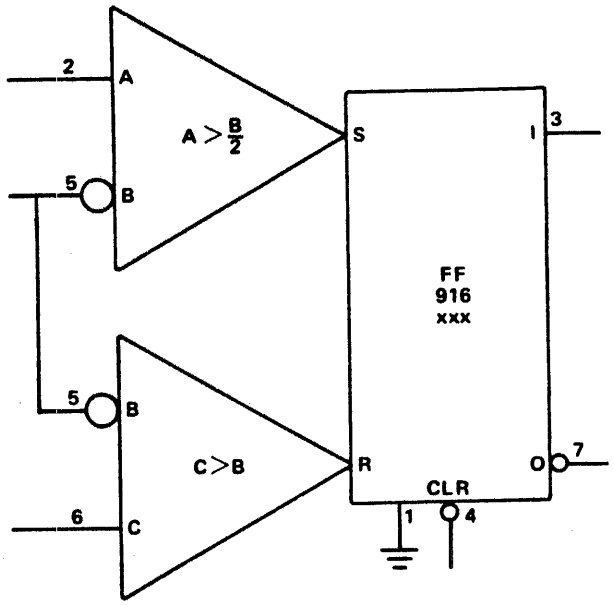
The 916 circuit may be used as a one-shot, a free-running multivibrator, or a comparator-input FF. Descriptions are provided for each of these applications.

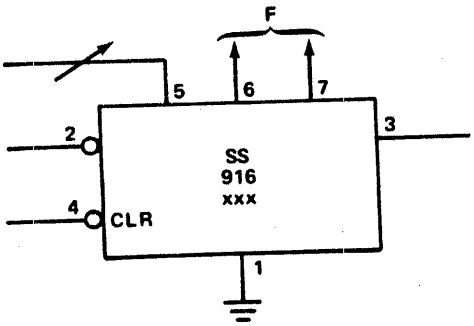
NOTES:

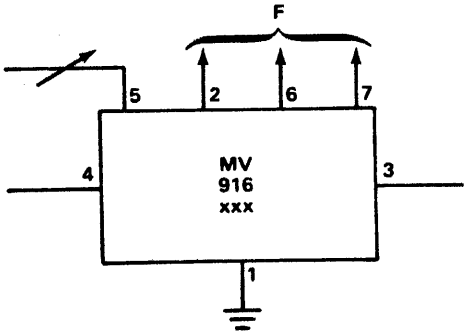
1. Vendor identification: NE555

2. Package pin configuration





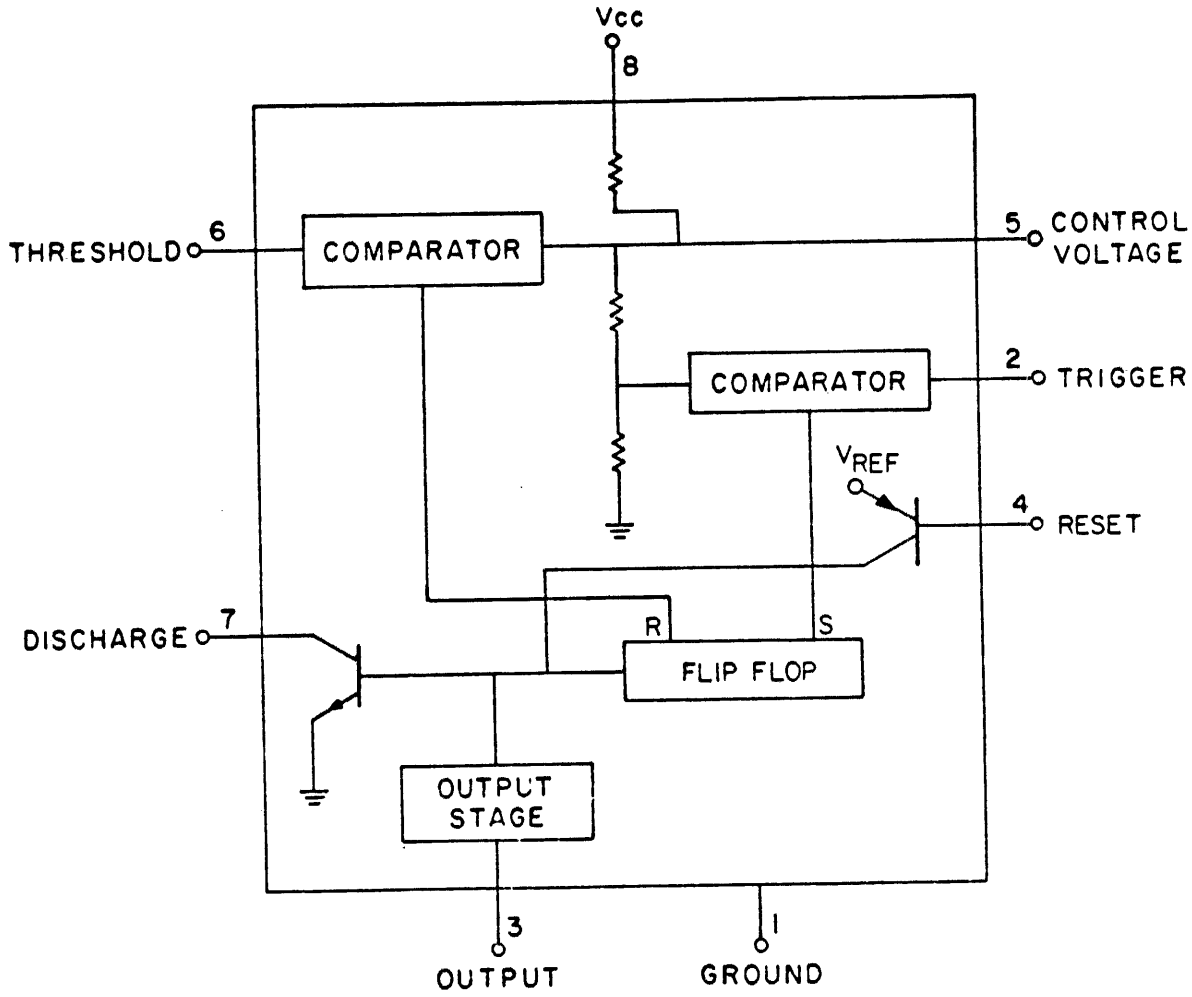




B = TO BIAS NETWORK
F = TO FREQ. COMPONENTS

Arrows in the line to pin 5 are omitted for fixed-frequency or fixed delay applications.

LOGIC SYMBOL



BLOCK DIAGRAM

916
Sheet 2 of 5

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Referring to Figure 1a, the external capacitor is initially held discharged by a transistor inside the timer.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set. This releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor now increases exponentially with the time constant $I = R_A C$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which, in turn, discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

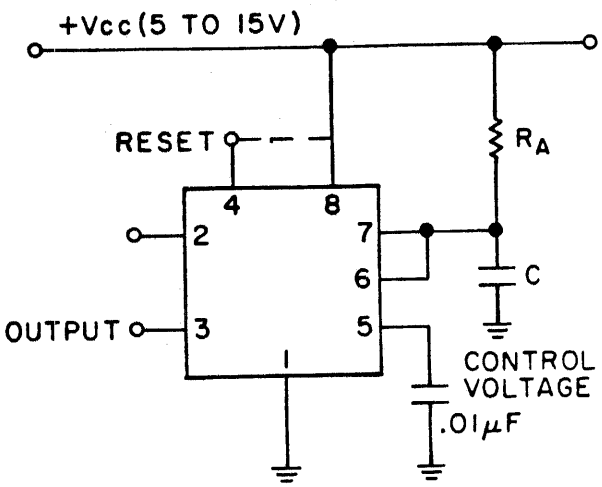


Figure 1a.

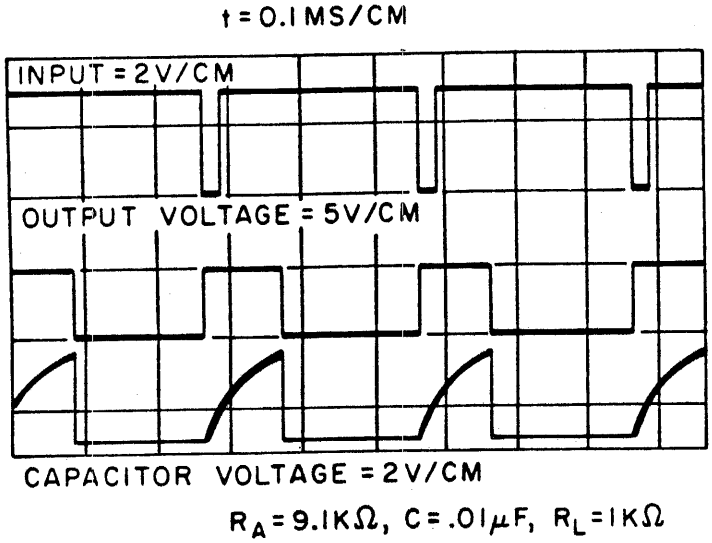


Figure 1b.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $T = 1.1 R_A C$. Because the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

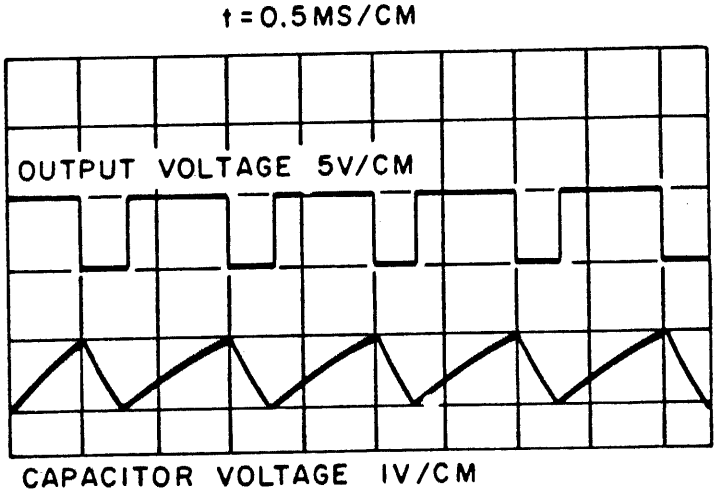


Figure 2b.

916
Sheet 4 of 5

Astable Operation

If the circuit is connected as shown in figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In this mode of operation, the capacitor charges and discharges between 1/3 C_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 2b shows actual waveforms generated in this mode of operation.

The charge timer (output high) is given by:

$$t1 = 0.693\ (R_A + R_B)\ C$$

and the discharge time (output low) by:

$$t2 = 0.693\ (R_B)\ C.$$

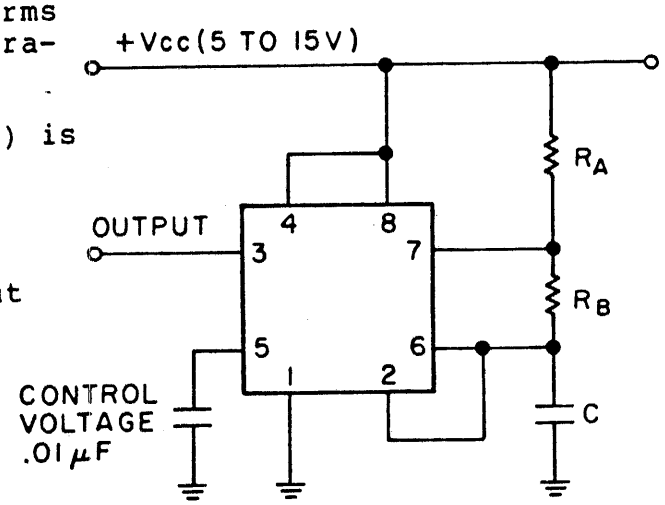


Figure 2a.

Comparator-Input Flip-Flop

This application is depicted by the top two symbol drawings on sheet 1. Pin 5 determines the quiescent voltage levels of the trigger (pin 2) and the threshold (pin 6). In practice:

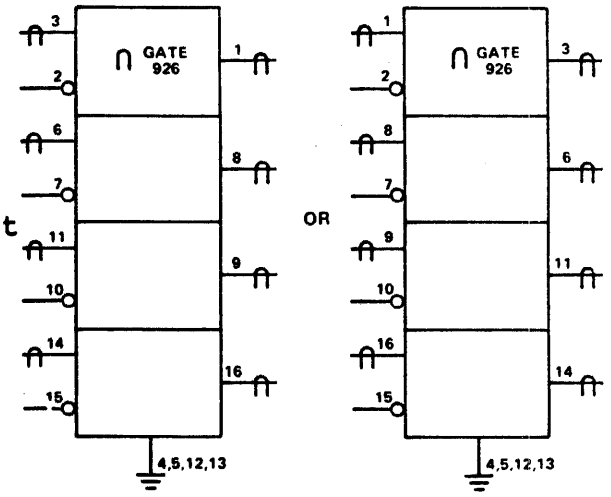
$$Vpin6 = Vpin5;\quad Vpin2 = \frac{Vpin5}{2}$$

When the level at pin 6 exceeds that at pin 5, the FF sets. When the level at pin 2 exceeds one-half of that at pin 5, the FF resets.

916
Sheet 5 of 5

DESCRIPTION

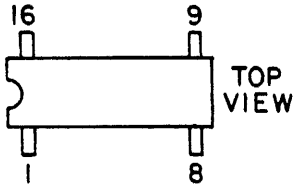
Element 926 is a bidirectional analog gate that switches on and off under the control of a binary input. A logic "0" turns the gate on and allows it to pass an analog signal from input to output. A logic "1" turns the gate off and causes it to block the analog signal.



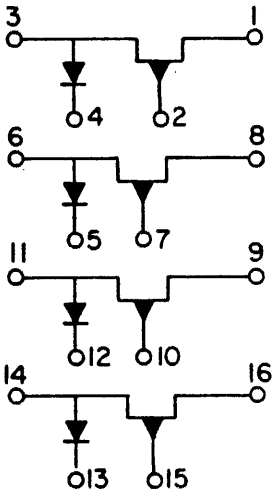
Pin	Function
3,6,11,14	Analog Inputs
1,8,9,16	Analog Outputs
2,7,10,15	Binary Inputs
4,5,12,13	Ground

NOTES:

1. Symbol sections may appear separately; show applicable ground pin for each section.
2. Vendor Identification: IH5012



PACKAGE PIN CONFIGURATION



FUNCTIONAL DIAGRAM

BINARY INPUT	FUNCTION
1	BLOCKS ANALOG SIGNAL
0	PASSES ANALOG SIGNAL

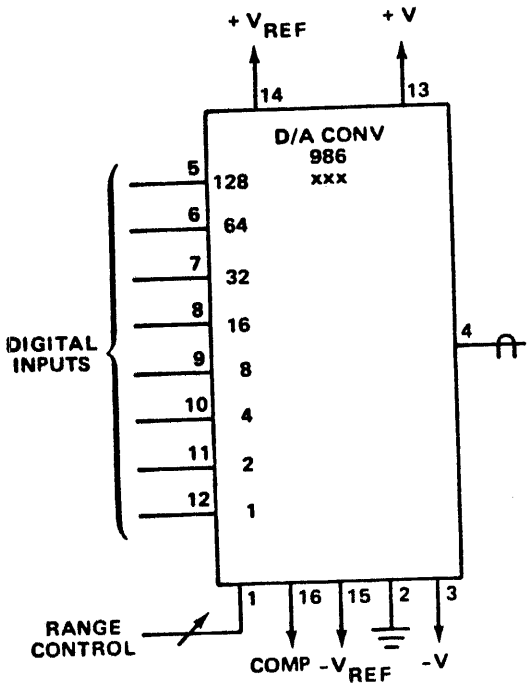
TRUTH TABLE

926
Sheet 1 of 1

DESCRIPTION

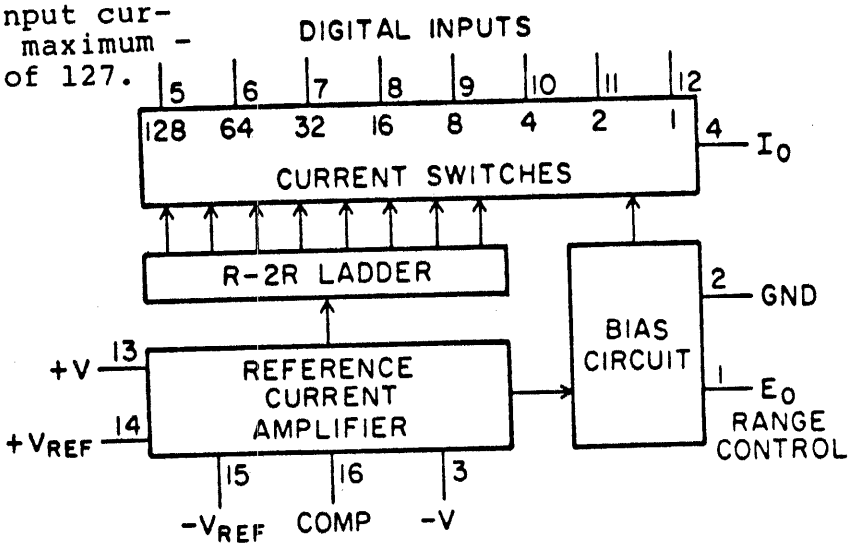
The 986 circuit is an eight-input digital-to-analog converter that provides its maximum output current (I_O) when all digital inputs are high (K=255), decreasing in discrete steps as the count goes from 255 to zero.

A reference current amplifier provides a constant current into the R-2R ladder, which divides the current into binary-related components that are fed to the current switches. Current from the reference amplifier is controlled by adjusting the positive/negative reference voltages. The output voltage (E_O) range may be varied by the voltage applied to pin 1. The compensation input, pin 16, maintains correct phase margin throughout the range.



LOGIC SYMBOL

The Typical Application diagram shows the 986 connected to provide 128 discrete output current values to an op amp (not part of the 986 circuit). The op amp feed-back resistor is selected to provide an E_O of 10 volts when input current to the op amp is maximum - that is, for a count of 127.



986
Sheet 1 of 2

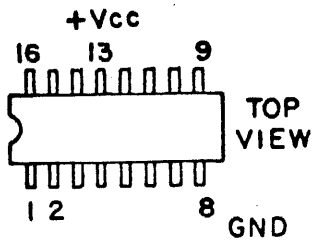
NOTES:

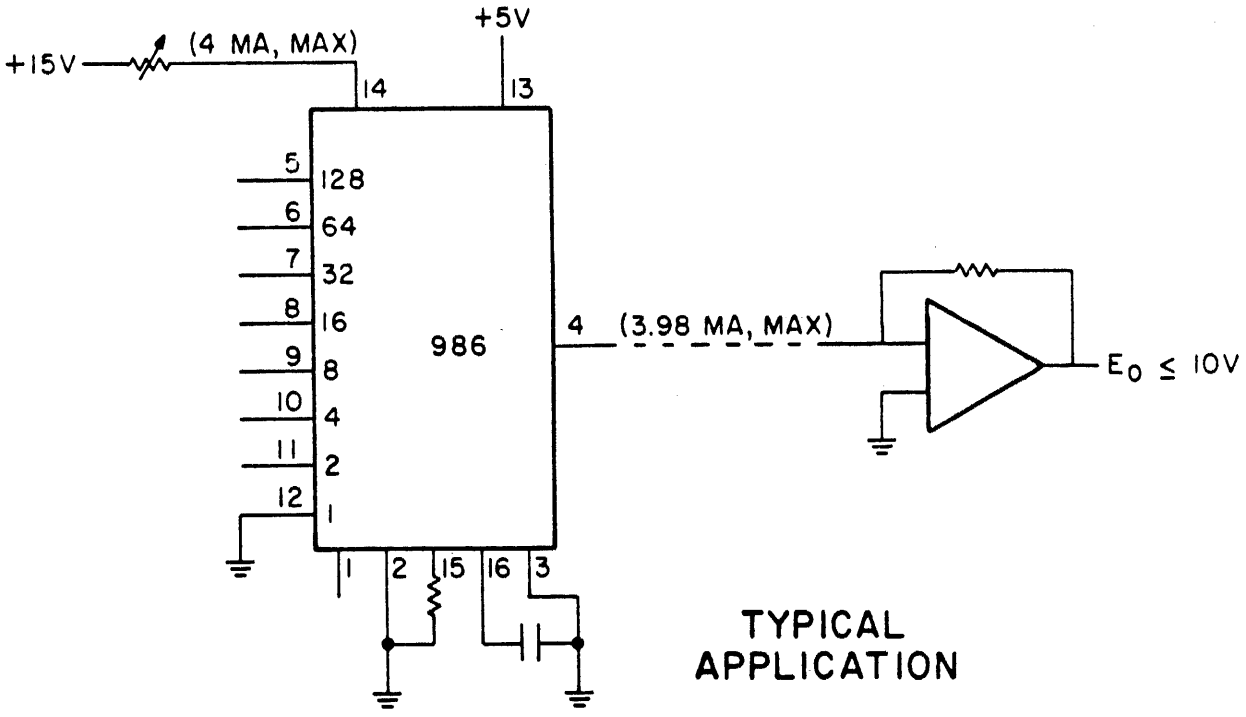
1. On a logic diagram, usually only the digital input and analog output pins are shown.

2. Vendor identification:

Element	Vendor Number
986A (6-Bit)	MC1408L-6
986B (7-Bit)	MC1408L-7
986D (8-Bit)	MC1408L-8
986E (8-Bit)	MC1408L-7.5

3. Package pin configuration.





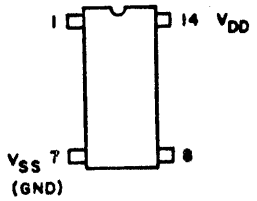
TYPICAL APPLICATION

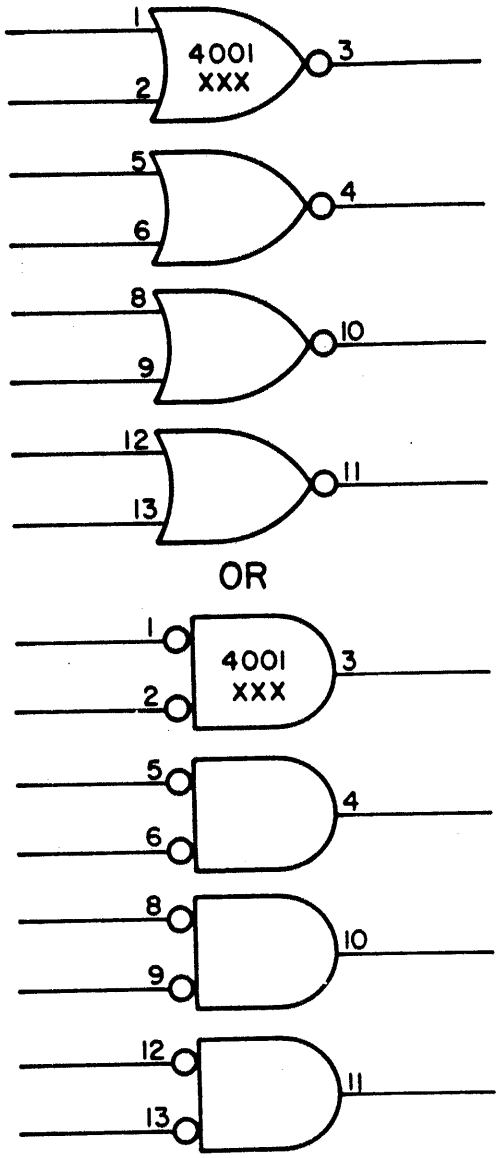
DESCRIPTION

The 4001 circuit is a CMOS package consisting of four 2-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4001
3. Package pin configuration:





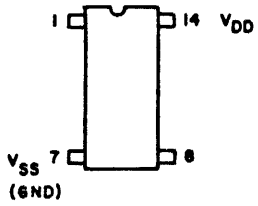
LOGIC SYMBOL

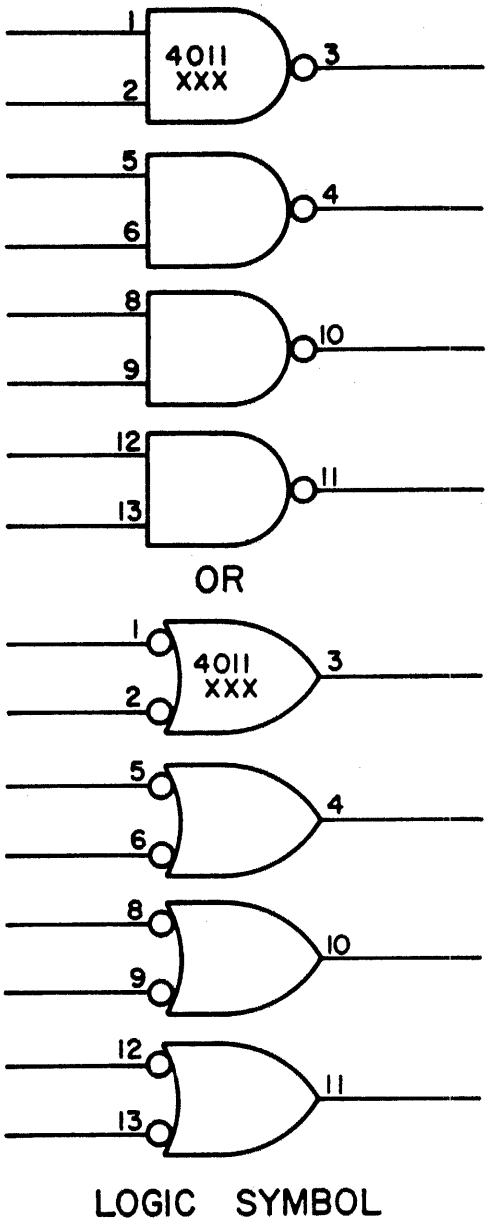
DESCRIPTION

The 4011 Circuit is a CMOS package consisting of four 2-input positive NAND gates.

NOTES:

1. Symbol sections may appear separately
2. Vendor identification: 4011
3. Package pin configuration:





LOGIC SYMBOL

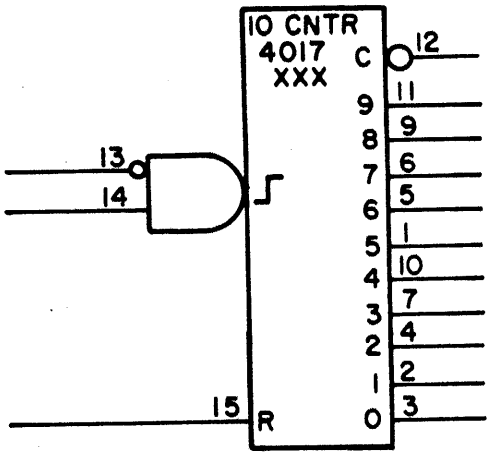
4011
Sheet 1 of 1

DESCRIPTION

The 4017 circuit is a CMOS decade counter with an asynchronous, active-high reset and a built-in count decoder. Changes in the output occur either on the positive-going edge of pin 14 provided that pin 13 is low or on the negative-going edge of pin 13 provided that pin 14 is high.

Outputs are normally low, going high only at the appropriate decimal count time.

A Carry output is provided that is high for all counts less than 5, and low for counts 5 through 9.

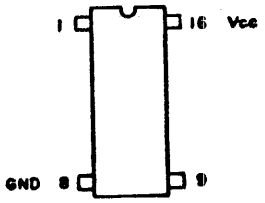


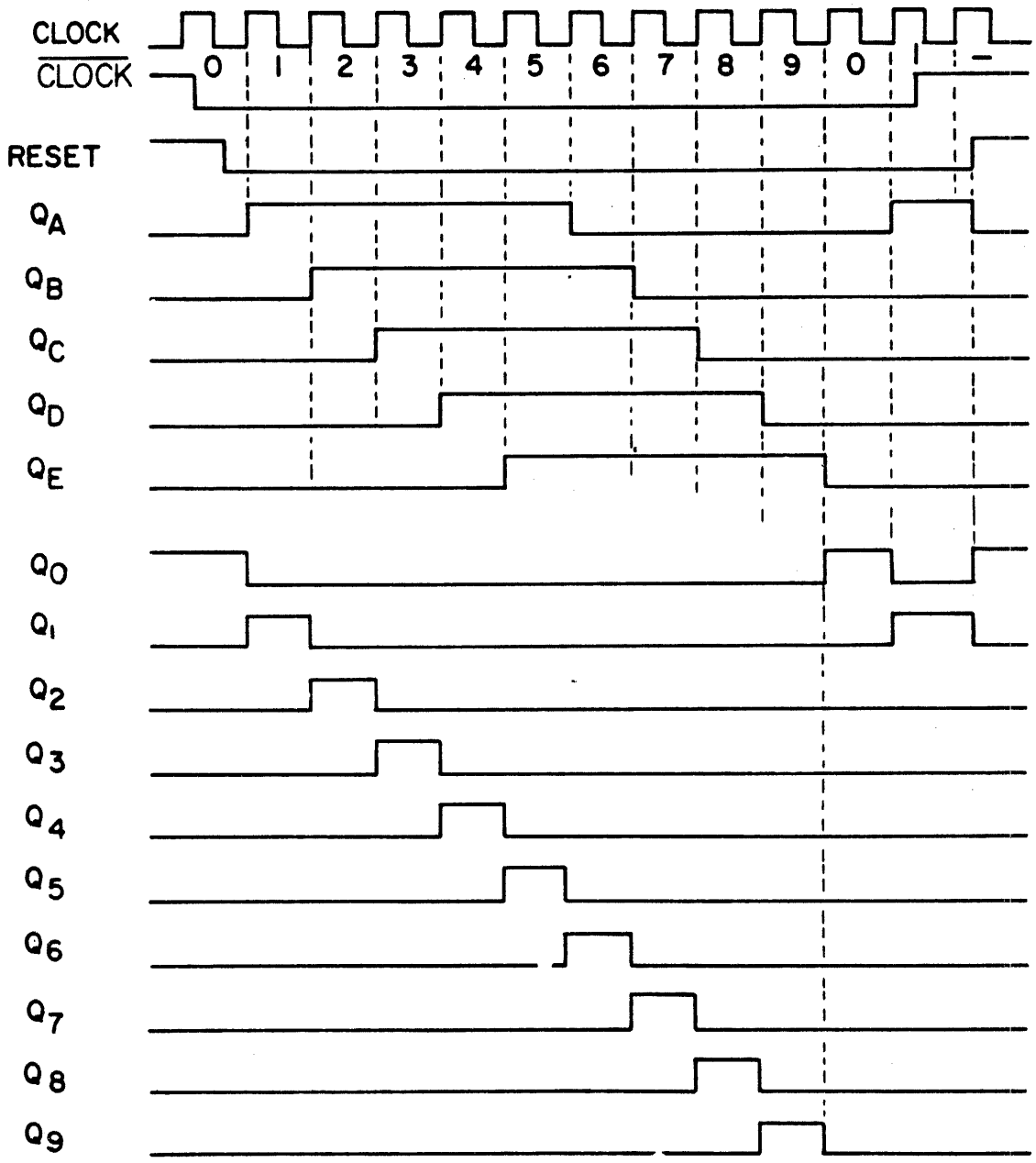
LOGIC SYMBOL

NOTES:

1. Vendor identification: 4017

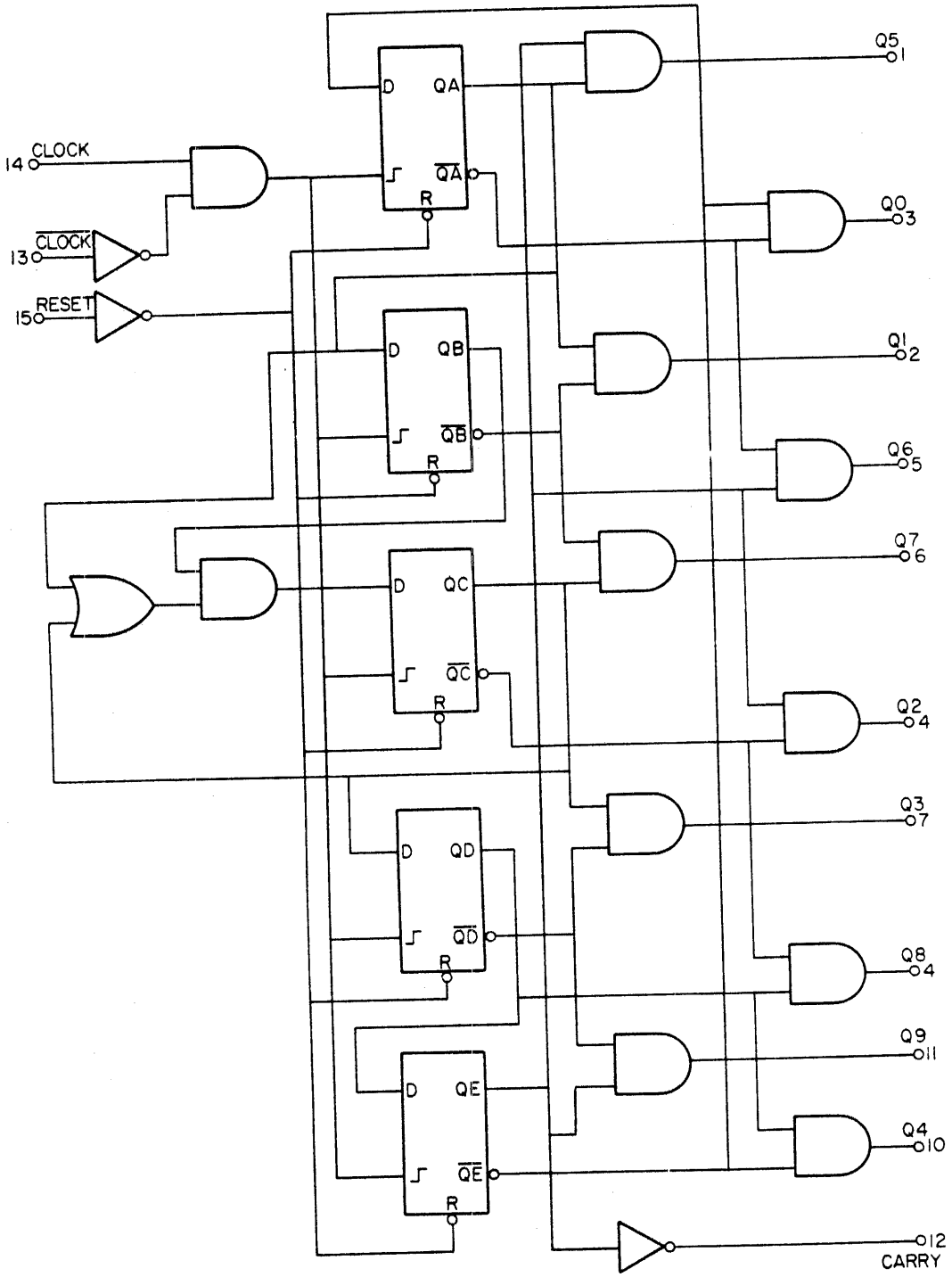
2. Package pin configuration:





TIMING DIAGRAM

4017
Sheet 2 of 3



FUNCTION DIAGRAM

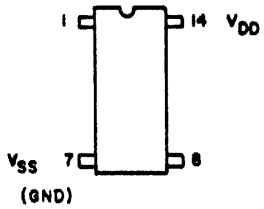
4017
Sheet 3 of 3

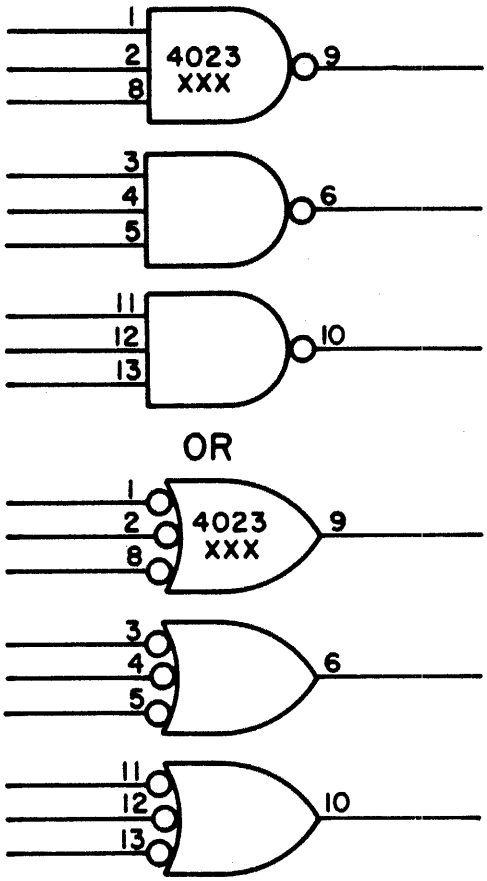
DESCRIPTION

The 4023 circuit is a CMOS package consisting of three 3-input positive NAND gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4023
3. Package pin configuration:





LOGIC SYMBOL

4023
Sheet 1 of 1

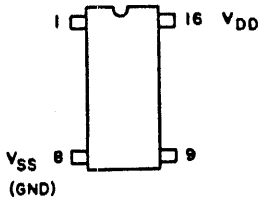
DESCRIPTION

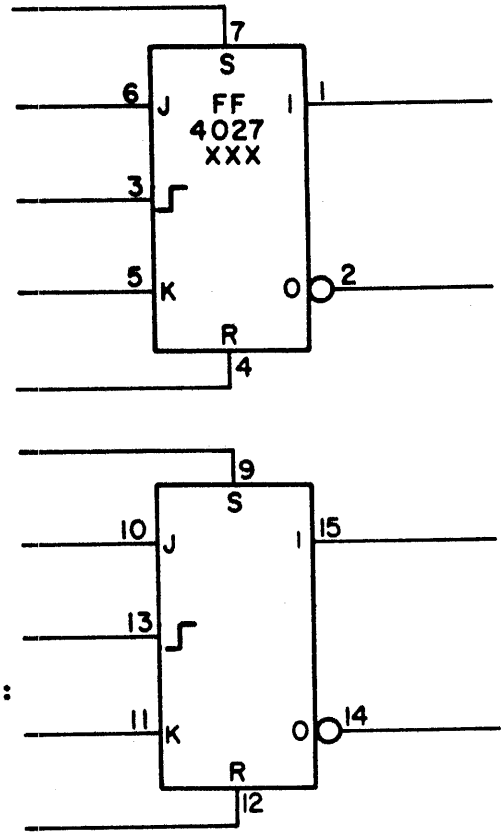
The 4027 circuit is a CMOS package consisting of two positive-edge-triggered J-K flip-flops with asynchronous set and clear inputs.

The functional (logic) diagram for the 4027 circuit appears as figure 4-15 in section 4A of this manual.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4027
3. Package pin configuration:





LOGIC SYMBOL

INPUTS					OUTPUT Qn+1		
G	GJ	GK	S	R	Q	$\overline{Q}$	
X	X	X	0	1	0	1	
X	X	X	1	0	1	0	
X	X	X	1	1	1	1	
⌐	0	0	0	0	Qn	$\overline{Qn}$	NO CHANGE
⌐	1	0	0	0	1	0	
⌐	0	1	0	0	0	1	
⌐	1	1	0	0	$\overline{Qn}$	Qn	TOGGLE

Qn = STATE OF Q OUTPUT PRIOR TO CLOCK TIME.

Qn + 1 = STATE OF OUTPUT AFTER CLOCK TIME.

⌐ = CLOCK TIME (L-TO-H TRANSITION)

X = DON'T CARE

TRUTH TABLE

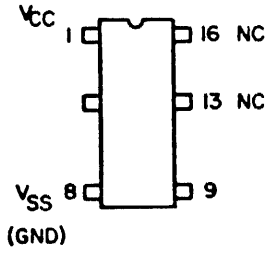
DESCRIPTION

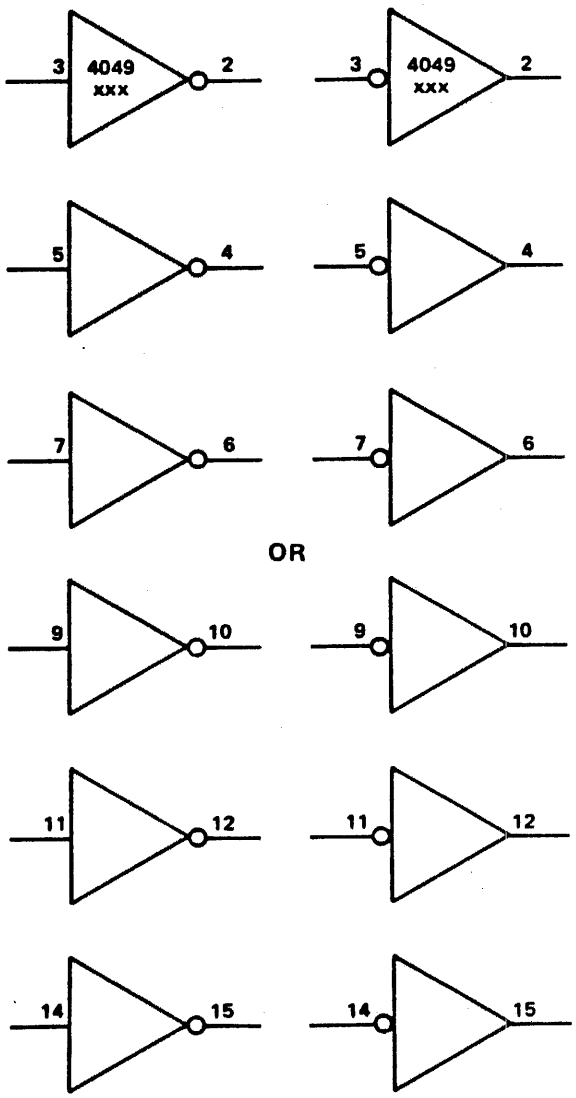
The 4049 circuit is a CMOS package consisting of six inverting buffers, each capable of driving up to two TTL loads when used as a CMOS-to-TTL converter. For that application, the high-level input voltage may exceed the TTL supply voltage (V_{CC}).

Pin 16 (normal V_{DD}) is not connected internally in this circuit, nor is pin 13.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4049
3. Package pin configuration:





4049
Sheet 1 of 1

DESCRIPTION

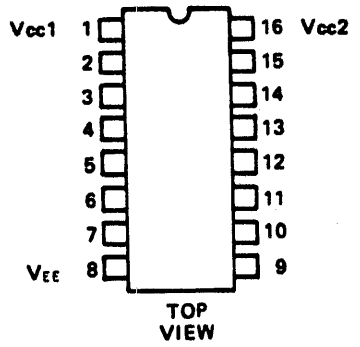
The 10102 is an ECL quad 2-input NOR gate. The last section provides complementary (OR/NOR) outputs.

NOTES:

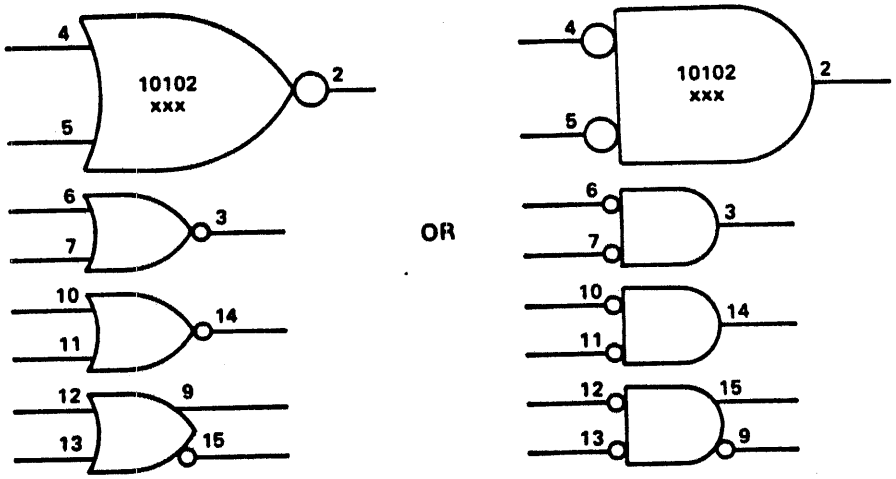
1. Vendor identification: MC10102L
2. Package pin configuration

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

TRUTH TABLE
(LAST SECTION)



TOP
VIEW



LOGIC SYMBOL

DESCRIPTION

The 10104 is an ECL quad 2-input AND gate. The last section provides complementary (AND/-NAND) outputs.

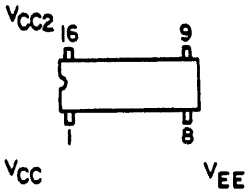
NOTES:

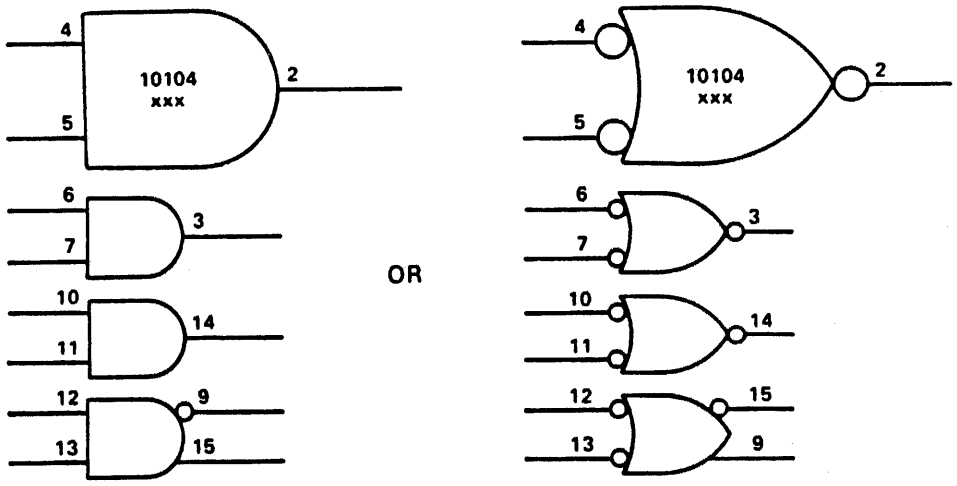
1. Vendor identification: MC10104L

2. Package pin configuration

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1

TRUTH TABLE
(LAST SECTION)

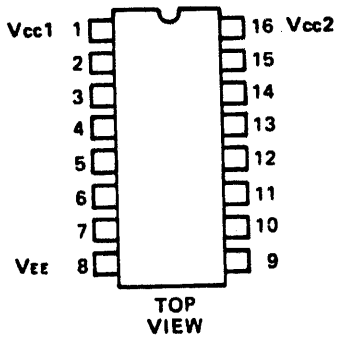




LOGIC SYMBOL

DESCRIPTION

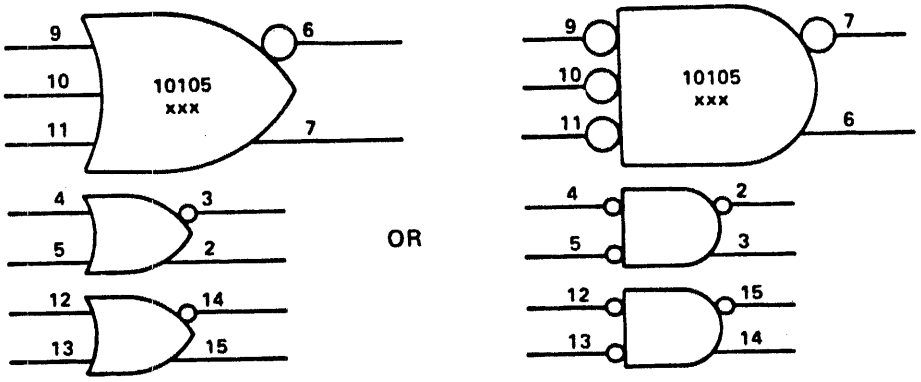
The 10105 is an ECL triple OR/NOR gate with a 3-2-2 input configuration. All sections provide complementary outputs.



NOTES:

1. Vendor identification: MC10105L

2. Package pin configuration.



LOGIC SYMBOL

10105
Sheet 1 of 1

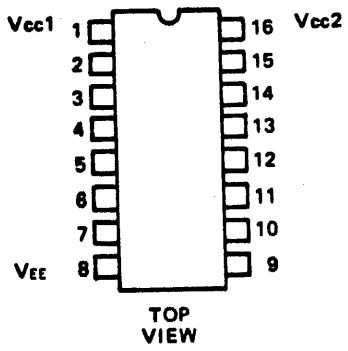
DESCRIPTION

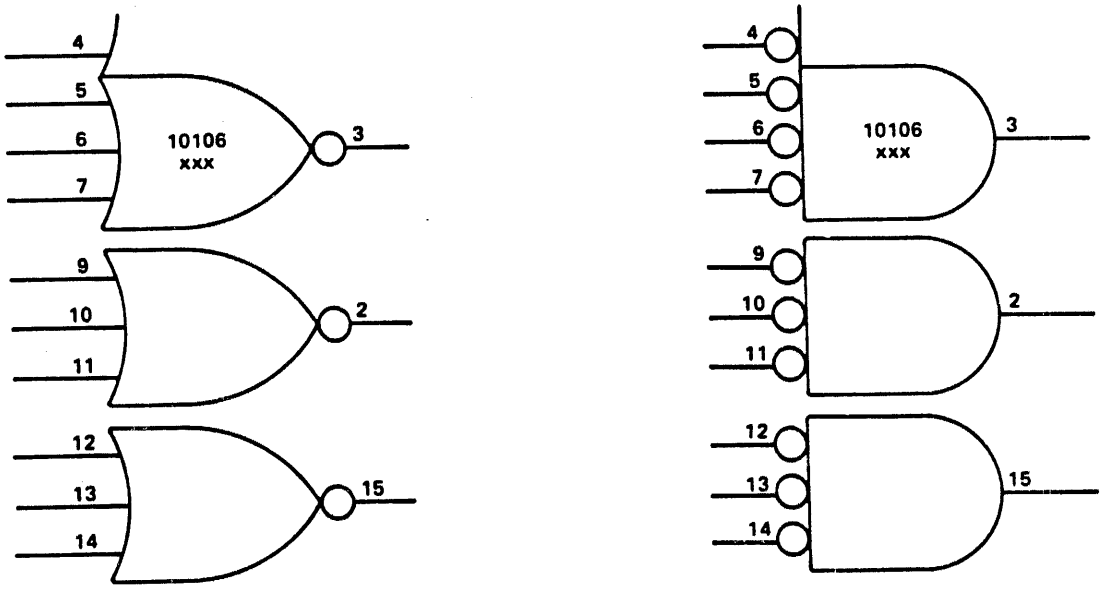
The 10106 is an ECL, triple, 4-3-3-input NOR gate.

NOTES:

1. Vendor identification: MC10106L

2. Package pin configuration:





LOGIC SYMBOL

10106
Sheet 1 of 1

DESCRIPTION

The 10116 is an ECL, triple differential line receiver. The line receivers are essentially very high speed linear differential amplifiers with standard ECL outputs.

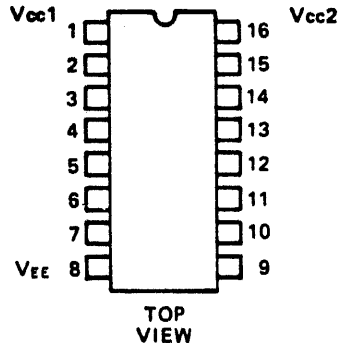
If any amplifier is unused, one input of that amplifier must be tied to V_{BB} (pin 11) to prevent upsetting the current source bias network.

NOTES:

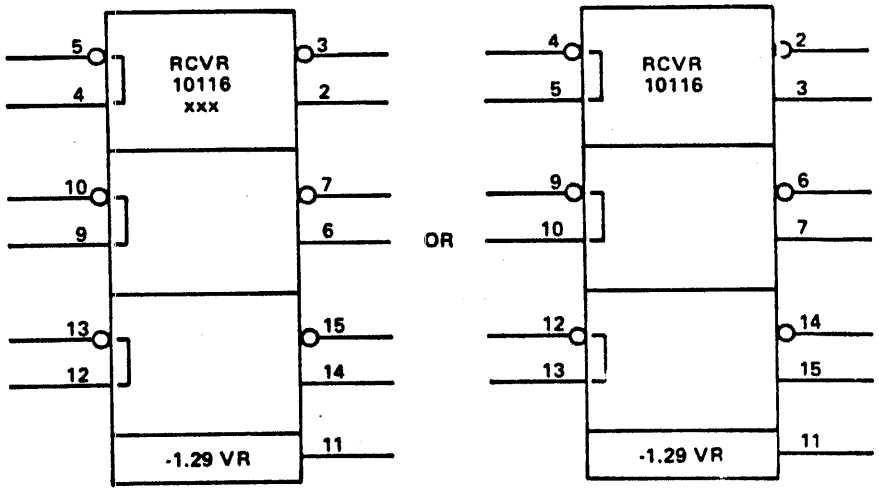
1. When sections are shown separately, the VR function (pin 11) is shown only with the last section.

2. Vendor identification: MC10116L

3. Package pin configuration:



TOP VIEW



LOGIC SYMBOL

10116
Sheet 1 of 1

DESCRIPTION

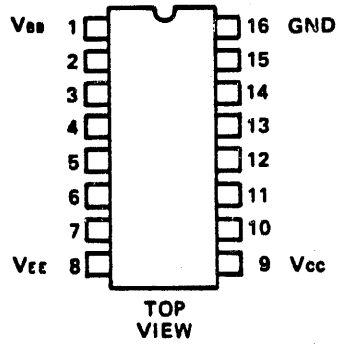
The 10125 is a quad ECL to TTL level translator.

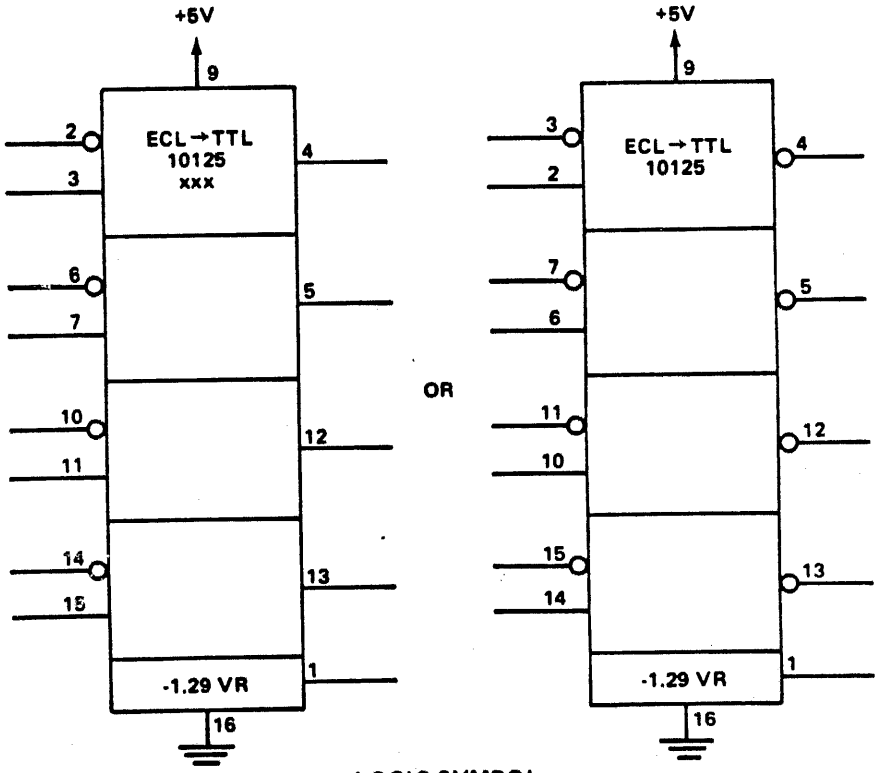
NOTES:

1. When sections are shown separately, the VR function (pin 1) is shown only with the last section. The ground (pin 16) is shown for each section, with the pin number in parentheses for the second, third, and fourth sections.

2. Vendor identification: MC10125L

3. Package pin configuration.





LOGIC SYMBOL

10125
Sheet 1 of 1

DESCRIPTION

The 10131 is an ECL circuit containing two master-slave, type-D FFs. The FFs are controlled either by the set and reset inputs or by the clock input used in conjunction with the D (data) input.

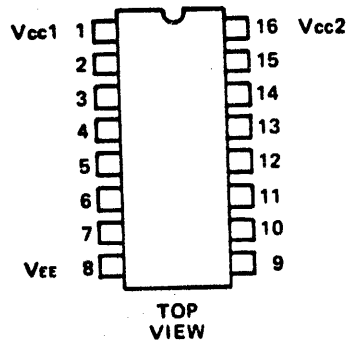
When both the set and reset inputs are low, the FFs are in the clocked mode and their output states change on the positive transition of the clock. The resulting change depends on the information present at the data (D) input.

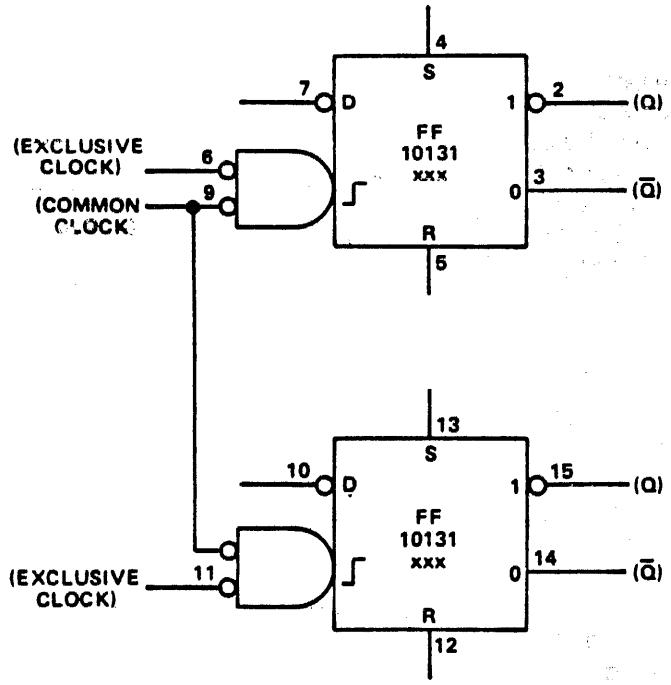
The FFs have both common and exclusive clock inputs. The FFs change separately, under control of their exclusive clock inputs, whenever the common clock input is held low. They change states simultaneously, under control of the common clock, whenever the exclusive clock inputs are held low. In either case, the final state of each FF depends on the information present at its data input at the time of the clock.

NOTES:

1. Vendor identification: MC10131

2. Package pin configuration:





LOGIC SYMBOL

TRUTH TABLES

INPUTS			OUTPUTS	
COMMON CLOCK	EXCLUSIVE CLOCK	DATA	Q	$\overline{Q}$
L	L	L	L	H
L	L	H	H	L
L	H	X	NC	NC
H	L	X	NC	NC
H	H	X	NC	NC

CLOCKED OPERATION

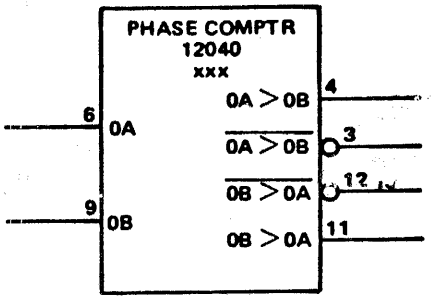
INPUTS		OUTPUTS	
SET	RESET	Q	$\overline{Q}$
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	ND	ND

SET/RESET OPERATION

H = HIGH L = LOW X = DON'T CARE
NC = No change from previous state
ND = Not Defined (Indefinite)

DESCRIPTION

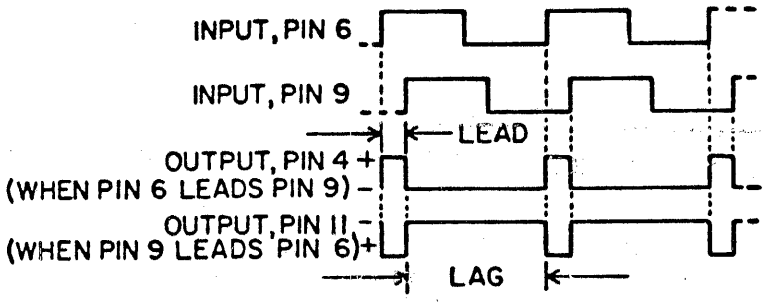
The 12040 is a logic network designed for use as a phase comparator for ECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms.



LOGIC SYMBOL

Operation of the 12040 is best described by assuming that two waveforms of the same frequency, but differing in phase, are applied to input pins 6 and 9 (see timing diagram). If the logic had established by past history that the waveform at pin 6 was leading the waveform at pin 9, the output of the comparator at pin 4 would be a positive pulse whose width is equal to the phase difference; and the output at pin 11 would remain low.

If the logic had established by past history that the waveform at pin 9 was leading the waveform at pin 6, the output of the comparator at pin 11 would be a positive pulse width equal to the phase difference; and the output at pin 4 would remain low.

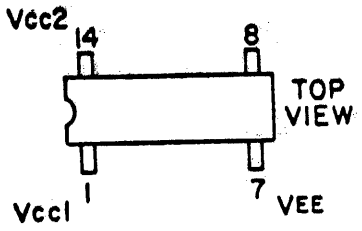


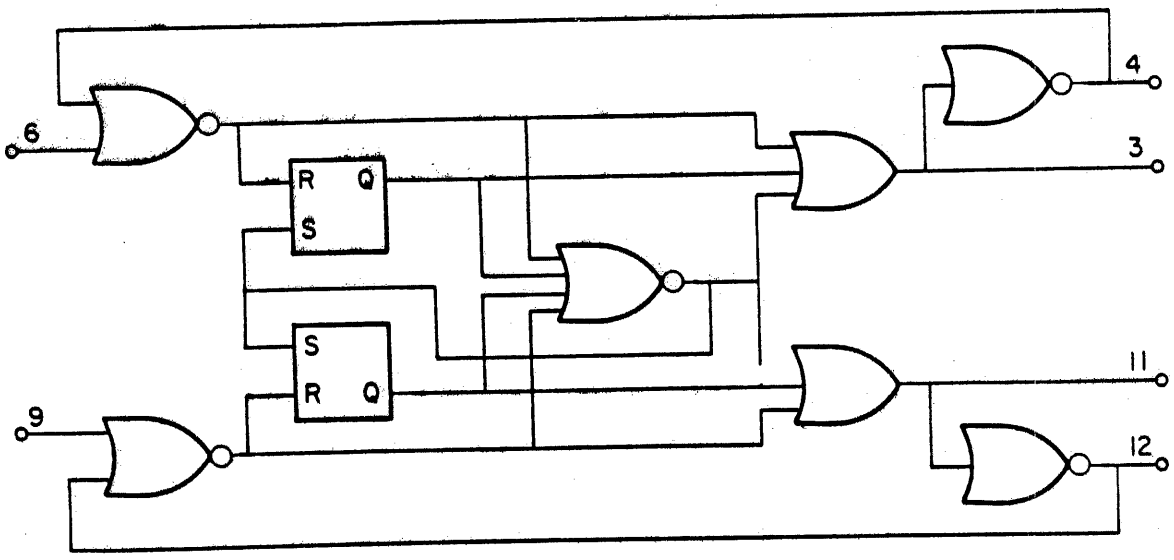
TIMING DIAGRAM

Both outputs for the sample condition are valid, since the determination of lead or lag is dependent on past edge crossings and initial conditions at start-up. A stable phase--locked loop will result from either condition. Phase error information is contained in the output duty cycle - that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the comparator, and by shifting the level to accommodate ECL swings, usable analog information for a voltage-controlled oscillator can be developed.

NOTES:

1. Vendor identification: MC12040
2. Package pin identification.





LOGIC DIAGRAM